Topics on Microelectronics (TOM) - http://www.innotechevents.com/ToM/Downloads/ToMCourses2018.pdf

September 19th, 2018 – University of Milan Bicocca

Optical Radio Frequency Integrated Circuits

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Something about the author

- Enrico Sacchi (https://www.linkedin.com/in/enrico-sacchi-1647a9/)
 - 1995: Laurea degree in Electrical Engineering (University of Pavia)
 - 1999: Electrical Engineering Ph.D. (University of Pavia) "Building Blocks for Highly Integrated CMOS RF Receivers"
 - 1999 2007: RFIC Design Engineer at STMicroelectronics (Pavia, Italy)
 - 2000 2001: Visiting Industrial Fellow at EECS Department, University of California at Berkeley
 - 2007 2017: Senior Design Engineer at Marvell (Pavia, Italy)
 - 2017 2018: Senior Design Engineer at Huawei Italia (Segrate, Mi)
 - 2018 ?: Principal Application Engineer at Cadence (Milano, Italy)





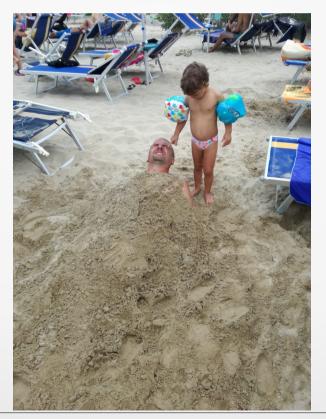






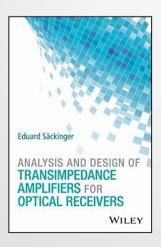
Silicon as a mission

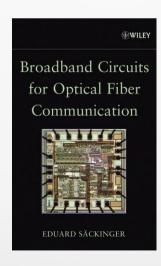
As you see, since my graduation thesis, silicon (CMOS) was always
the focus of my working life. Also during vacation time I like to "play"
with it, even if in the beach sand, silica (SiO₂) is not pure as it should
be and it is mixed with calcium carbonate

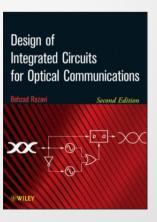


Acknowledgment (1/2)

- Hisilicon Team @ Huawei Italia, for the great job carried out together
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 Julio Lonac, Luca Piazzon, Antonio Musio, Danilo Caccioli,
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- Cadence Italia, for allowing me to keep this lecture today
- Edward Säckinger and Behzad Razavi for their great books







Acknowledgment (2/2)







- The Free Software Foundation, the GNU project and the open source software movement. With the exception of Cadence Tools, everything used to arrange this presentation is "open-source"
 - OS: Linux (Mint) on the PC and Linux (RedHat) on the servers
 - Slides: Libreoffice Impress
 - Images: Inkscape and Gimp
 - PDF viewer: Evince
 - Search engine: Duck-Duck-Go















Outline

- (Short) Introduction to Optical Communications
- Broadband Techniques
- Optical RFICs
 - Transimpedance Amplifier (TIA)
 - Modulator Driver
- Conclusions

Motivation

- Light-wave communications is a necessity for the information age
- Optical links provide enormous bandwidth and the optical fiber is the only medium that can meet the modern society need for transporting massive amount of data over long distances
 - Global high capacity networks, which constitute the backbone of the Internet
 - Massive parallel interconnects that provide data connectivity inside data-centers and supercomputers

Multi-discipline

Cooperation between

- Experts in photonics
- Experts in communications
- Experts in electronics
- Experts in signal processing

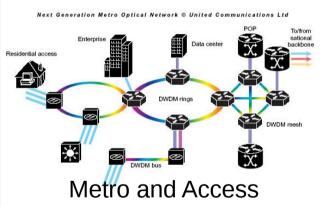
Common goal

- Always increasing demand for higher capacity
- Lower costs
- Lower energy consumptions

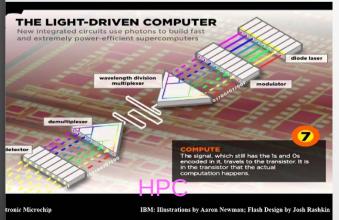
Fiber-optic communications

 Exponentially increasing data consumption is expanding the applications of optical communication and driving the development of faster and more efficient transceivers









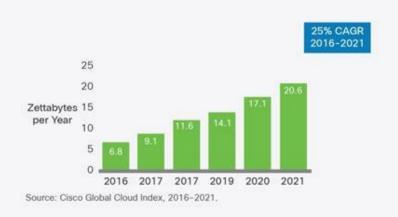


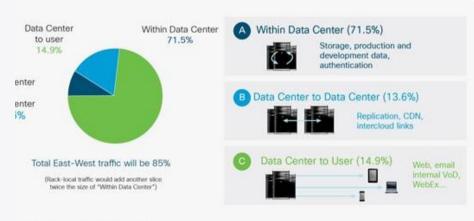


Traffic data exponential growth (1/3)



- Cloud services (Google, Amazon, Microsoft, Dropbox, Baidu...)
 - Annual global data center IP traffic will reach 20.6 zettabytes **Dropbox** (ZB), by the end of 2021, up from 6.8 ZB per year in 2016
 - By 2021, 94 percent of workloads and compute instances will be processed by cloud data centers; 6 percent will be processed by traditional data centers





: Cisco Global Cloud Index, 2016-2021.

Traffic data exponential growth (2/3)

- 5G Wireless: it is the next generation of mobile networking technology following 4G. Like every generation before it, 5G aims to make mobile communication faster and more reliable as more and more devices go on-line
 - HD-streaming smart-phones, watches with data plans, always-on security cameras, self-driving and Internet-connected cars, augmented reality hardware
- Multimedia streaming
 - Netflix, Youtube, Hulu, Spotify









Traffic data exponential growth (3/3)

amazon

• E-Commerce: Amazon, Ebay, Alibaba





- Big Data: this term tends to refer to the use of predictive analytics, user behavior analytics, or certain other advanced data analytics methods that extract value from data, and seldom to a particular size of data set
- Social: Facebook, Instagram



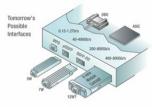


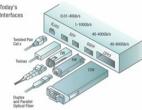
 IoT: fast growing constellation of internet-connected sensors attached to a wide variety of "things". Sensor can take a multitude of possible measurements, thus generating data and traffic

MEDIA AND MODULES

Ethernet is wired technology and supports a variety of media including backplanes, twisted pair, twinax, multimode fiber and single-mode fiber. Most people know Ethernet by the twisted pair or Cat "x" cabling with RJ45 connectors because close to a billion ports a year are sold.

The graphic below shows multiple types of modules that may be used for copper or optical links. The upper modules are being developed to support ultra-high density port counts. The µOSFP shrinks the QSFP down to an SFP size while the QSFP-DD doubles the lane count to 8. On Board Optics (OBO) enable the highest port counts on switches.





2016

ETHERNET ROADMAP

THE PAST, PRESENT AND FUTURE OF ETHERNET



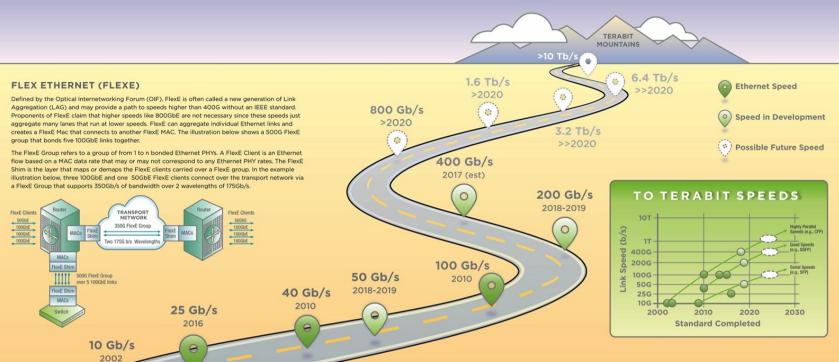


www.ethernetalliance.org

Designed by Scott Kipp

Ethernet Alliance 2016. All rights reserved.

2016 ETHERNET ROADMAP



5 Gb/s

2.5 Gb/s 2016

1 Gb/s

100 Mb/s 1995

10 Mb/s 1983

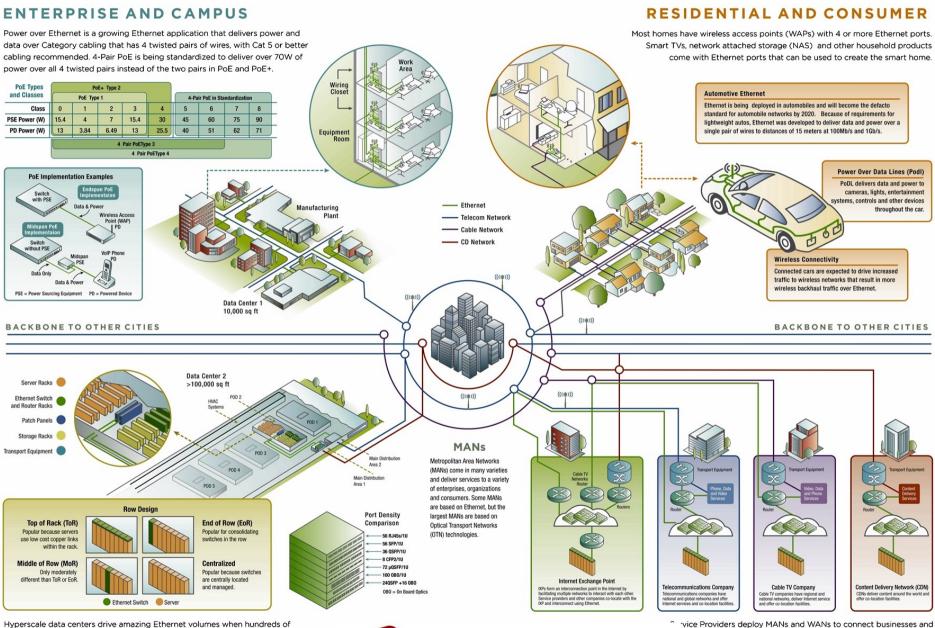
ETHERNET INTERFACES AND NOMENCLATURE

	Electrical Interface	Backplane	Twinax Cable	Twisted Pairs	MMF	Parallel SMF	2km SMF	10km SMF	40km SMF
10BASE-				Т					
100BASE-				TX	FX			LX	
1000BASE-		кх	сх	Т	SX			LX	
2.5GBASE-		кх		Т					
5GBASE-		KR		Т					
10GBASE-	SFI, XFI	KX4, KR	CR	Т	SR			LR	ER
25GBASE-	25GAUI	KR	CR	Т	SR			LR	ER
40GBASE-	XLAUI	KR4	CR4	Т	SR4		FR	LR4	ER4
50GBASE-	50GAUI (-2?)	KR	CR		SR		FR	LR	
100GBASE-	CAUI10	KR4, KR2	CR10,		SR10	PSM4	10X10	LR4	ER4
	CAUI4		CR4,		SR4		CWDM4	10X10	10X10
	CAUI-2		CR2		SR2		CLR4		
200GBASE-	200GAUI-4	KR4	SR4		SR4		FR4	LR4	
400GBASE-	CDAUI-16				SR16	DR4	FR8	LR8	
	CDAUI-8								

Gray Text = IEEE Standard Red Text = In Standardization Green Text = Under consideration in IEEE

Blue Text = Non-IEEE standard but complies to IEEE electrical interfaces

ETHERNET ECOSYSYTEM



HYPERSCALE DATA CENTER

thousands of servers are connected on one site.



consumers. Some carriers deploy hyperscale data centers as well

SERVICE PROVIDERS

Optical Standards

- IEEE and Optical Internetworking Forum (OIF) are the two entities that provide the standardization for optical communications
- Ethernet standard (IEEE 802.3), written and maintained by IEEE, includes all the communications example we will talk through the presentation. It is a very articulated standard
 - IEEE 802.3a (1985) 10Base-2 (thin ethernet)
 - IEEE 802.3i (1990) 10Base-T (twisted pair)
 - IEEE 802.3ab (1999) 1000Base-T (gigabit ethernet over twisted pair)
 - IEEE 802.3ae (2002) 10-Gigabit Ethernet
- Standardization cover all the aspects:
 - Physical layer (connectors, like SMF) and medium (fiber)
 - Modulations (NRZ or PAM4, for example)

Optical fibers evolution (1/2)

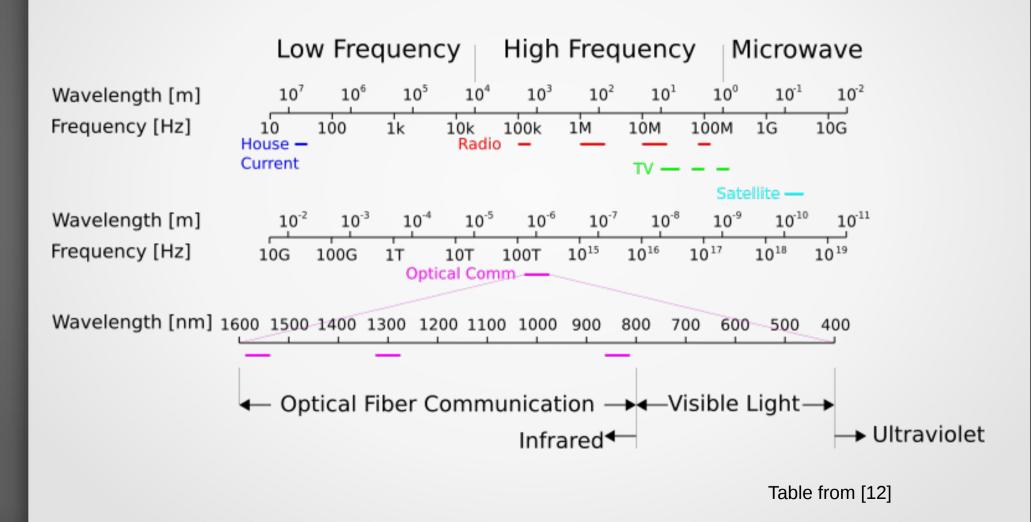
- 1966: Vision and predictions of ultra-low loss silica glass
 - Kao K.C. and Hockman A., "Dielectric-Fiber surface waveguides for optical frequencies", Proc IEE vol 113
- 1970: First demonstration of < 20 dB/Km optical fiber loss
 - Kapron F.P., Kerk D. B., Maurer R.D., "Radiation losses in glass optical waveguides", Appl Phys Letters, vol 17
- 1977: the first live telephone traffic was transmitted through multi-mode fiber by GTE (@ 6 Mb/s) and AT&T (@ 45 Mb/s)

Optical fiber evolution (2/2)

- Dense Wavelength Division Multiplexing (DWDM): it has the capability to send multiple signals on the same fiber, using different wavelength
 - Up to 10 Tb/s of traffic per single fiber
 - Distance more than 1000 km
 - Example: 2000000 simultaneous Netflix HD stream in a wire smaller than a human hair (!!!)
- As a drawback, the link becomes more complex
 - Target distance
 - Chromatic dispersion
 - Optical signal to noise ratio (OSNR)

https://www.prolabs.com/wp-content/uploads/2016/06/White-Paper-Understanding-DWDM.pdf

Optical frequencies

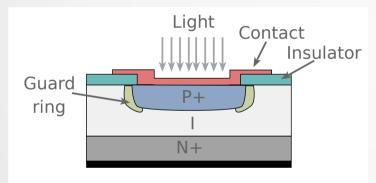


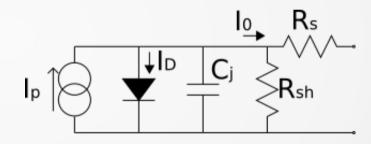
Technology for Optical RFICs

- Like it happened, in early '90, for the so-called RF, the ever growing volume of data in telecommunication networks has pushed interest in high-speed optical and electronic devices and systems
 - Modular, general-purpose building blocks have been gradually replaced by end-to-end solutions that benefit from device/circuit/architecture co-design
 - Mainstream VLSI technologies such as CMOS and BiCMOS continue to take over the territories thus far claimed by GaAs and InP device
 - Silicon Photonics

Photodiodes (1/3)

 Silicon photodiodes are semiconductor devices responsive to high-energy particles and photons. Photodiodes operate by absorption of photons or charged particles and generate a flow of current in an external circuit, proportional to the incident power.





PIN photodetector

• The current source I_p generated by the incident radiation, and the diode represent the p-n junction. In addition, a junction capacitance (C_j) and a shunt resistance (R_{SH}) are in parallel with the other components. Resistance (R_S) is connected in series with all components in this model

Photodiodes (2/3)

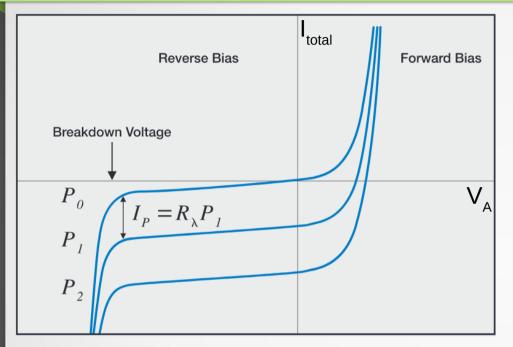
- Photodetector characteristics
 - **Responsivity**: it is a measure of the sensitivity to light, and it is defined as the ratio of the photocurrent I_p to the incident light power P at a given wavelength:

$$R_{\lambda} = \frac{I_p}{P}$$

I-V Characteristic: The current-voltage characteristic of a photodiode with no incident light is similar to a rectifying diode. When the photodiode is forward biased, there is an exponential increase in the current. When a reverse bias is applied, a small reverse saturation current appears. It is related to dark current as:

$$I_d = I_{sat}(e^{\frac{q V_A}{k_B T}} - 1)$$

Photodiodes (3/3)



 Illuminating the photodiode with optical radiation, shifts the I-V curve by the amount of photocurrent (I_P). Thus

$$I_{total} = I_{sat} \left(e^{\frac{qV_A}{k_B T}} - 1 \right) - I_P$$

- Noise: in a photodiode two sources of noise can be identified
 - Shot noise: statistical fluctuation of both I_d and I_P

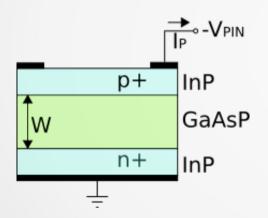
$$I_{sn} = \sqrt{2q(I_p + I_d)\Delta f}$$

• Thermal noise: thermal generation of carriers

$$I_{th} = \sqrt{\frac{4 k T \Delta f}{R_{sh}}}$$

Photodiodes typologies (1/2)

- P-i-n photodetector
 - it consists of a p-n junction with a layer of intrinsic (undoped or lightly doped) semiconductor material sandwiched. The junction is reverse biased (-V_{PIN})

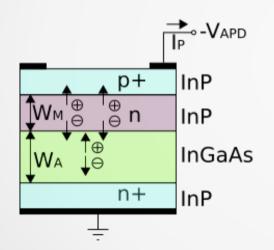


 P-i-n photodetector bandwidth (speed) depends on the width of the absorption layer W, the reverse bias V_{PIN}, its capacitance and packaging

 Vertically illuminated p-i-n are normally used for applications up to 10 Gbps. More sophisticated p-i-n (edge-coupled) are used for higher speeds

Photodiodes typologies (2/2)

- Avalanche photodetector
 - As the p-i-n, it is a reverse biased diode, with an additional layer (multiplication region) providing internal gain through avalanche multiplication



 The gain of the APD is called multiplication factor (M)

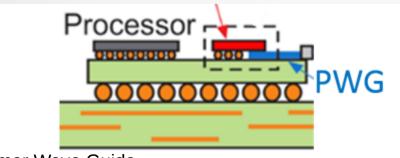
$$i_{APD} = MRP = R_{APD}P$$

$$R_{APD} \approx 10 A/W$$

 The APD provides also more noise than p-i-n PD. Such amount of noise is (not linearly) dependent on the avalanche gain → there is an optimum for best sensitivity

Silicon Photonics (1/2)

- Photonic Integrated Circuits (PICs) is an emerging technology that uses crystalline semiconductor wafers as the platform for the integration of active and passive photonic circuits along with electronic components on a single micro-chip.
- Integrated photodetectors
 - Bringing the photodetector as close as possible to the TIA and avoiding separate packages reduces total capacitance at TIA input node (better noise and speed as we will see....)





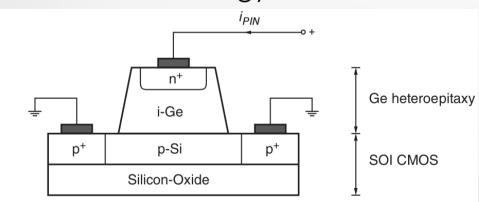


Courtesy from

https://www.zurich.ibm.com/st/photonics/adiabatic.html

Silicon Photonics (2/2)

- The Receiver Optics Sub-Assembly (ROSA), made by PD,
 TIA and optical components can be integrated in different ways
 - Detector (InP) and circuit chip (CMOS or SiGe or GaAs) in the same package, as a Multi Chip Module
 - Detector chip (InP) mounted on the circuit chip (CMOS or Sige or GaAs) through flip chip or bondwire
 - Detector and circuit monolithically integrated in a standard circuit technology

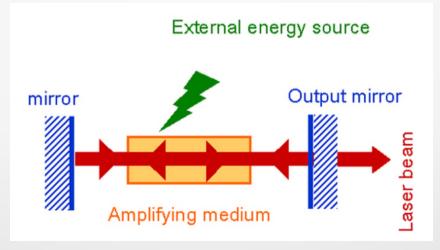


Selective hetero-epitaxy to grow germanium detector on top of an SOI wafer

- R = 0.9 A/W
- Dark current: 300 nA

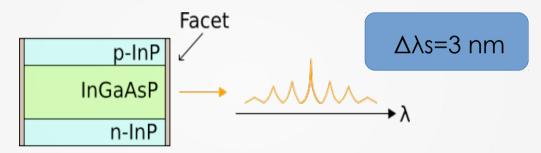
Laser

- The word laser is an acronym of Light Amplification by Stimulated Emission of Radiation. Lasers are devices that produce or amplify a beam of narrow, low-divergence light with a well-defined wavelength.
- In data communications, the Fabry-Perot (FP) and the Vertical-Cavity Surface-Emitting Laser (VCSEL) are mostly used to generate a modulated optical signal



Fabry-Perot Laser

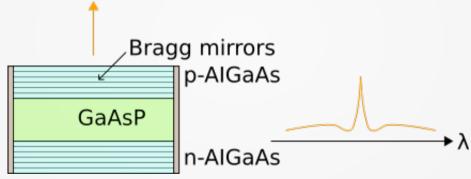
 The Fabry-Perot laser consists of an optical gain medium located in a cavity formed by two reflecting facets.



- Forward biased p-n junction injecting carriers (electrons and holes) into a thin active region: these carriers "pump" the active region such that an incoming photon can stimulate the recombination of an electron-hole pair to produce a second photon (gain)
- Both 1.3 μ and 1.5 μ can be based on an InGaAsP active layer

Vertical-Cavity Surface-Emitting Laser

 The VCSEL emits the light perpendicular to the wafer surface, rather than at the edges of the chip. It consists of a gain medium located in a very short vertical cavity (1 µm) with Bragg mirrors at the bottom and the top



- Bragg mirrors are formed by many layers of alternating high and low reflective index material
- Low cost: commercially available at short wavelength (0.85 µm band) where fiber loss is appreciably high

Coherent optical communications

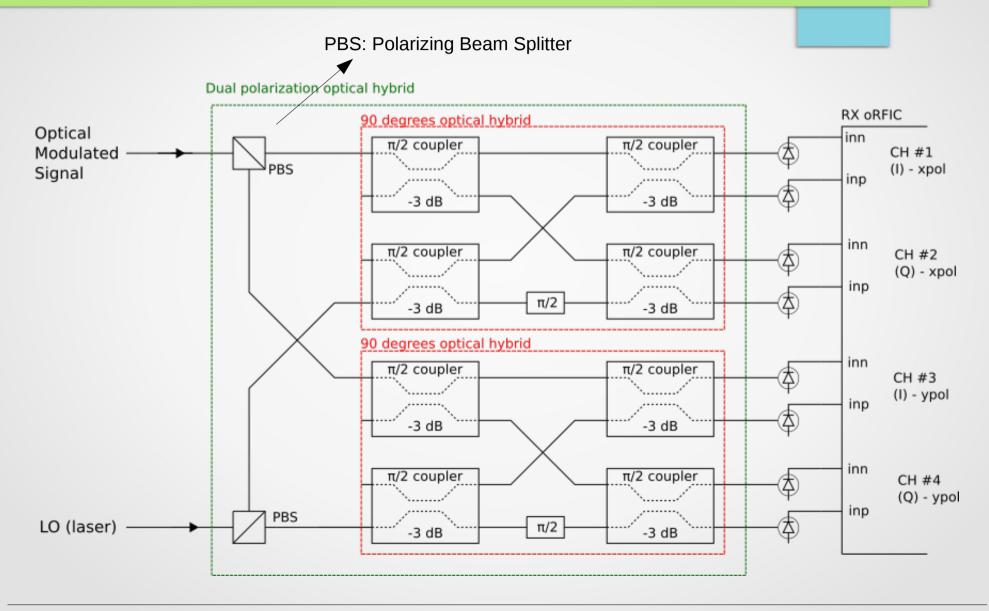
- The first optical fiber communications systems (late '70s, '80s) used intensity modulation of semiconductor lasers, and the intensity of the optical signal transmitted through an optical fiber was detected by a photodiode
 - These systems are called IM-DD (Intensity Modulation and Direct Detection)
 - Receiver sensitivity is dependent neither on the carrier phase nor on the state of polarization of the incoming signal
 - Still widely used
- On the other hands, a receiver (RX) in which the signal is interfered with a Local Oscillator (LO) so as to extract the phase information of the signal is called a coherent RX
 - Heterodyne and homodyne RX belongs to this category

IM-DD vs Coherent

	Coherent	IM-DD		
Modulation parameters	I&Q - Amplitude and Phase	Intensity		
Decision method	Heterodyne or homodyne	Direct Detection		
Sensitivity to carrier phase	yes	no		
Sensitivity to polarization	yes	no		

- As its most basic, coherent optical transmission is a technique that uses modulation of the amplitude and phase of the light, as well as transmission across two polarizations, to enable the transport of considerably more information through a fiber optic cable.
- Using Digital Signal Processing (DSP) at both transmitter and receiver, coherent optics also offers higher bit-rates, greater degrees of flexibility, simpler photonic line systems, and better optical performance

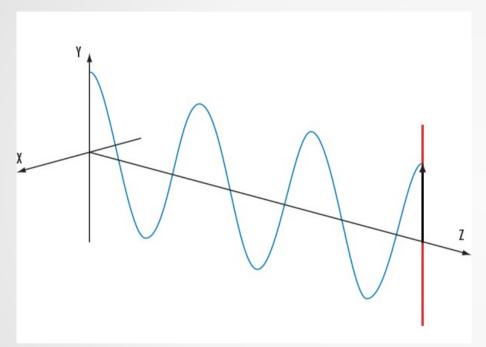
Coherent Optical RX FE (1/2)

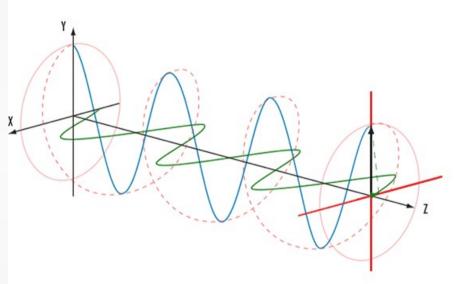


Coherent Optical RX FE (2/2)

- The modulated optical signal has two orthogonal polarizations, each carrying a separate data path
 - The signal beam is split through a polarizing beam splitter (PBS) into two X-polarized and Y-polarized beams and sent to two identical opto-electrical front-ends
- Laser is split by a beam-splitter (BS) and sent to the two identical receive path as local oscillator (LO)
- The cascade of the 90 degrees optical hybrid and the two balanced photodiode (PD) pairs performs the quadrature downconversion of the modulated signal
 - A total of 4 receive channels are implemented inside the oRFIC: I
 + Q for X-pol optical signal and I+Q for the Y-pol optical signal

Single and orthogonal polarization

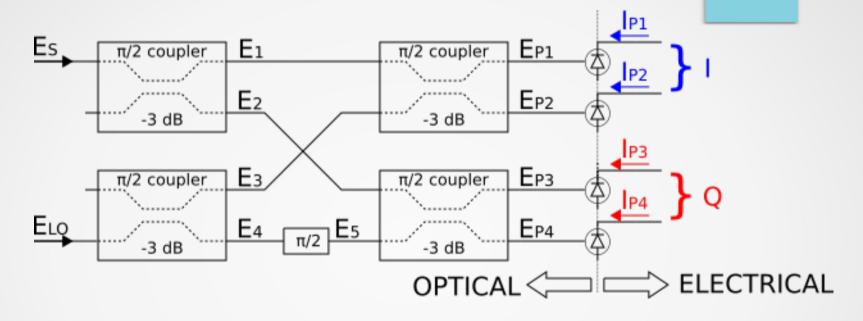




The electric field of linearly polarized light is confined to a single plane along the direction of propagation.

The electric field of circularly polarized light consists of two perpendicular, equal in amplitude, linear components that have a phase of difference of $\pi/2$. The resulting electric field describes a circle.

90 degrees optical hybrid



- "E" are electric fields, "I" are currents
- E_{LO} is unmodulated, with an unknown phase: $E_{LO} = |E_{LO}| e^{j\theta_{LO}}$
- E_s is modulated, with a time-varying phase and constant amplitude (assuming QPSK): $E_s = |E_s| e^{j\theta_s(t)}$

Calculations - Optical domain

$$E_{1} = \frac{E_{S}}{\sqrt{2}}$$

$$E_{2} = \frac{jE_{S}}{\sqrt{2}}$$

$$E_{2} = \frac{jE_{LO}}{\sqrt{2}}$$

$$E_{3} = \frac{jE_{LO}}{\sqrt{2}}$$

$$E_{4} = \frac{E_{LO}}{\sqrt{2}}$$

$$E_{5} = \frac{-jE_{LO}}{\sqrt{2}}$$

$$E_{5} = \frac{-jE_{LO}}{\sqrt{2}}$$

$$E_{7} = \frac{E_{1} + jE_{3}}{\sqrt{2}} = \frac{1}{2}(jE_{S} + jE_{LO})$$

$$E_{1} = \frac{E_{1} + jE_{3}}{\sqrt{2}} = \frac{1}{2}(jE_{S} + jE_{LO})$$

$$E_{2} = \frac{jE_{1} + E_{3}}{\sqrt{2}} = \frac{1}{2}(jE_{S} + E_{LO})$$

$$E_{2} = \frac{jE_{2} + jE_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{1} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{2} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{2} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{jE_{2} + E_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{jE_{2} + iE_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{jE_{2} + iE_{5}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{3} = \frac{iE_{1} + jE_{3}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{4} = \frac{iE_{1} + jE_{3}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{5} = \frac{iE_{1} + iE_{3}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

$$E_{5} = \frac{iE_{1} + iE_{3}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

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$$E_{5} = \frac{iE_{1} + iE_{3}}{\sqrt{2}} = \frac{1}{2}(-E_{S} - jE_{LO})$$

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PD currents (1/2)

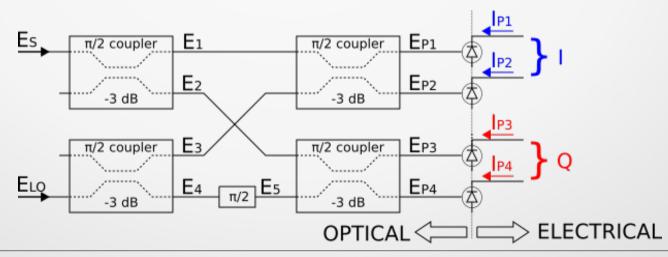
$$I_{P1} = \rho |E_{P1}|^2 = \frac{\rho}{4} (|E_S|^2 + |E_{LO}|^2 - 2\Re(E_S E_{LO}^*))$$

$$I_{P2} = \rho |E_{P2}|^2 = \frac{\rho}{4} (|E_S|^2 + |E_{LO}|^2 + 2 \Re (E_S E_{LO}^*))$$

$$I_{P3} = \rho |E_{P3}|^2 = \frac{\rho}{4} (|E_S|^2 + |E_{LO}|^2 - 2\Im(E_S E_{LO}^*))$$

$$I_{P4} = \rho |E_{P4}|^2 = \frac{\rho}{4} (|E_S|^2 + |E_{LO}|^2 + 2\Im(E_S E_{LO}^*))$$

p is the photodiode responsivity [A/W]



PD currents (2/2)

• Using:
$$E_{LO} = |E_{LO}| e^{j\theta_{LO}} E_S(t) = |E_S| e^{j\theta_S(t)} P_S = |E_S|^2 P_{LO} = |E_{LO}|^2$$

$$\begin{split} I_{P1} &= \rho \big(\frac{P_S}{4} + \frac{P_{LO}}{4} - \frac{\sqrt{P_S P_{LO}}}{2} \cos \big(\theta_S(t) - \theta_{LO} \big) \big) \\ I_{P2} &= \rho \big(\frac{P_S}{4} + \frac{P_{LO}}{4} + \frac{\sqrt{P_S P_{LO}}}{2} \cos \big(\theta_S(t) - \theta_{LO} \big) \big) \\ I_{P3} &= \rho \big(\frac{P_S}{4} + \frac{P_{LO}}{4} - \frac{\sqrt{P_S P_{LO}}}{2} \sin \big(\theta_S(t) - \theta_{LO} \big) \big) \\ I_{P4} &= \rho \big(\frac{P_S}{4} + \frac{P_{LO}}{4} + \frac{\sqrt{P_S P_{LO}}}{2} \sin \big(\theta_S(t) - \theta_{LO} \big) \big) \end{split}$$

DC current (common to all PD)

$$I_{DC} = \rho \left(\frac{P_S}{4} + \frac{P_{LO}}{4} \right)$$

AC diff curr I-path (I_{P1} - I_{P2})

$$I_{I} = \rho \sqrt{P_{S} \cdot P_{LO}} \cos(\theta_{s}(t) - \theta_{LO})$$

AC diff curr Q-path (Ip3 - Ip4)

$$I_Q = \rho \sqrt{P_S \cdot P_{LO}} \sin(\theta_s(t) - \theta_{LO})$$

Comments

- If $P_{LO} >> P_S$, DC current does not depend on the input signal's power
 - A small AC current and a large DC current can coexist at sensitivity
- In principle, DC current is the same on all PDs and it is proportional to the sum of the LO and Signal optical power
 - In practice, a significant mismatch among the photo-diodes can exist, so a DC differential current can occur
- Optical losses on LO path (α_{LO}) and signal path (α_s) (in addition to the 3 dB attenuations of the couplers) can be taken into account

$$I_{DC} = \rho \left(\frac{\alpha_{S} \cdot P_{S}}{4} + \frac{\alpha_{LO} \cdot P_{LO}}{4} \right)$$

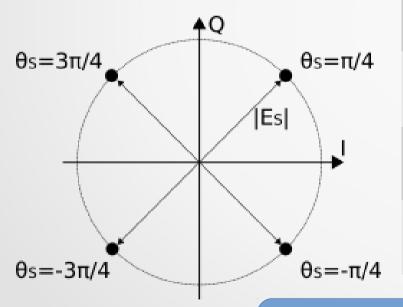
$$I_{Q} = \rho \sqrt{\alpha_{S} P_{S} \cdot \alpha_{LO} P_{LO}} \sin \left(\theta_{s}(t) - \theta_{LO} \right)$$

$$I_{Q} = \rho \sqrt{\alpha_{S} P_{S} \cdot \alpha_{LO} P_{LO}} \sin \left(\theta_{s}(t) - \theta_{LO} \right)$$

QPSK Modulation and PD currents (1/2)

 LO phase is unknown. Here are two scenarios, giving min/max peakto-peak differential current at TIA inputs in the case of QPSK modulation

- Case 1:
$$\theta_{LO}$$
=0

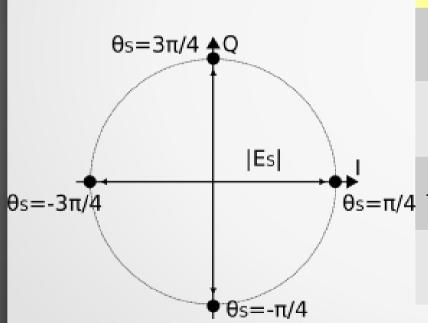


θ_{S}	$I_{_I}$	I_Q
$\pi/4$	$\frac{\rho}{\sqrt{(2)}}\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$	$\frac{\rho}{\sqrt{(2)}}\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$
$\frac{-\pi}{4}$	$\frac{\rho}{\sqrt{(2)}}\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$	$\frac{-\rho}{\sqrt{(2)}}\sqrt{(\alpha_{S}P_{S}\cdot\alpha_{LO}P_{LO})}$
$\frac{-3}{4}\pi$	$\frac{-\rho}{\sqrt{(2)}}\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$	$\frac{-\rho}{\sqrt{(2)}}\sqrt{(\alpha_{S}P_{S}\cdot\alpha_{LO}P_{LO})}$
$\frac{3}{4}\pi$	$\frac{-\rho}{\sqrt{(2)}}\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$	$\frac{\rho}{\sqrt{(2)}}\sqrt{(\alpha_{S}P_{S}\cdot\alpha_{LO}P_{LO})}$

$$I_{pkpkdiff} = \sqrt{(2)} \rho \sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$$

QPSK Modulation and PD currents (2/2)

Case 2: $\theta_{LO} = \pi/4$

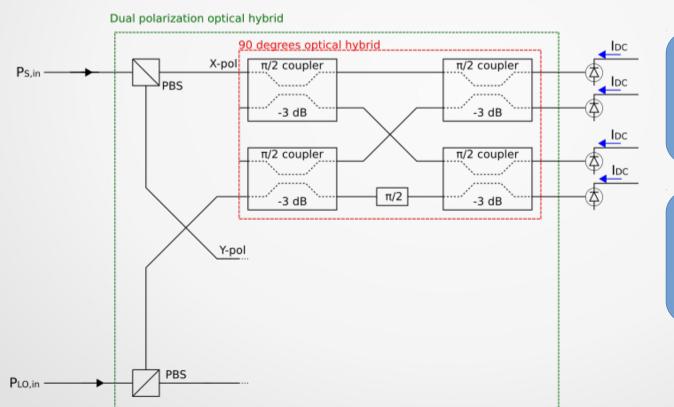


Θ_S	I_{I}	I_Q
$\pi/4$	$\rho\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$	0
$\frac{-\pi}{4}$	0	$-\rho\sqrt{(\alpha_{S}P_{S}\cdot\alpha_{LO}P_{LO})}$
$\frac{-3}{4}\pi$	$-\rho\sqrt{(\alpha_{S}P_{S}\cdot\alpha_{LO}P_{LO})}$	0
$\frac{3}{4}\pi$	0	$\rho\sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$

$$I_{pkpkdiff} = 2 \rho \sqrt{(\alpha_S P_S \cdot \alpha_{LO} P_{LO})}$$

Optical losses and measurements (1/2)

 A way to evaluate the optical losses is to measure the signal and LO paths separately



$$P_{\sin} = P_i, P_{LOin} = 0$$
$$I_{DC,S} = \frac{\rho}{4} \alpha_S P_i$$

$$P_{\sin} = 0, P_{LOin} = P_i$$

$$I_{DC,LO} = \frac{\rho}{4} \alpha_{LO} P_i$$

(same for all PDs)

Optical losses and measurements (2/2)

 Optical losses on LO and signal path can be calculated from measured quantities

$$\alpha_{S} = \frac{I_{DC,S}}{P_{i}} \cdot 4 \cdot \frac{1}{\rho}$$

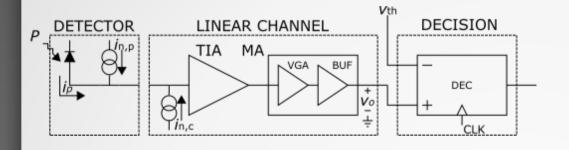
$$\alpha_{LO} = \frac{I_{DC,LO}}{P_{i}} \cdot 4 \cdot \frac{1}{\rho}$$
PD responsivity [A/W]

Whole path measured responsivity [A/W]

Receiver fundamentals

- Receiver sensitivity: how noise in the receiver causes bit errors
- Bit Error Rate (BER)
- Noise Bandwidth
- Optical Signal-to-Noise ratio (OSNR)
- Intersymbol Interference (ISI)
- Noise and ISI trade-off

Basic receiver model



- P: optical power
- R: PD responsivity
- i_p=R P (proportional to optical power!!!)
- i_{n,p}= detector noise
- H(f): Linear channel freq response
- i_{n c}: circuit noise
- Photodiode (PD) current i_p is linearly proportional to optical power
 P!!!
- PD noise i_{n,p} is depending on the photodiode impedance !!!
- i_{n,p}: white, non stationary, non-Gaussian
- i_{n,c}: frequency dependent, stationary, Gaussian

$$i_{n,c}^2(f) = a_0 + a_2 f^2$$

(still to be demonstrated)

Noise and bit-error rate

- $\vee_{0}(\dagger) = \vee_{s}(\dagger) + \vee_{n}(\dagger)$
 - v_s(t): desired output signal voltage
 - v_n(t): output noise voltage originated from both circuits (mainly TIA) and PD
- Both output signal voltage and output noise voltage are time-dependent and it may happen that, at a given time instant, (maybe at ts, when the decision circuit has to "choose" between 0 and 1) that v_n(ts) is not negligible compared to v_s(ts), and the decision circuit makes a mistake

Output noise

$$\begin{aligned} V_{n,c}^2(f) &= |H(f)|^2 \times I_{n,c}^2(f) \end{aligned} \qquad \text{(Circuit noise output PSD)} \\ \bar{v}_{n,c}^2 &= \int_0^{BW,d} |H(f)|^2 \times I_{n,c}^2(f) \, df \qquad \text{(Circuit noise output power)} \\ \bar{v}_{n,p}^2 &= \int_0^{BW,d} |H(f)|^2 \times I_{n,p}^2(f,t)(f) \, df \qquad \text{(PD noise output power)} \end{aligned}$$

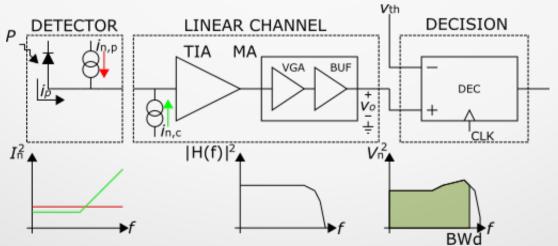
 From the noise output power it is possible to calculate the rms noise voltage at the output

$$v_{n,p}^{rms}(t) = \sqrt{\int_{0}^{BW,d} |H(f)|^2} \times [I_{n,c}^2(f) + I_{n,p}^2(f,t)(f)] df$$

BW,d: Bandwidth of the decision circuit

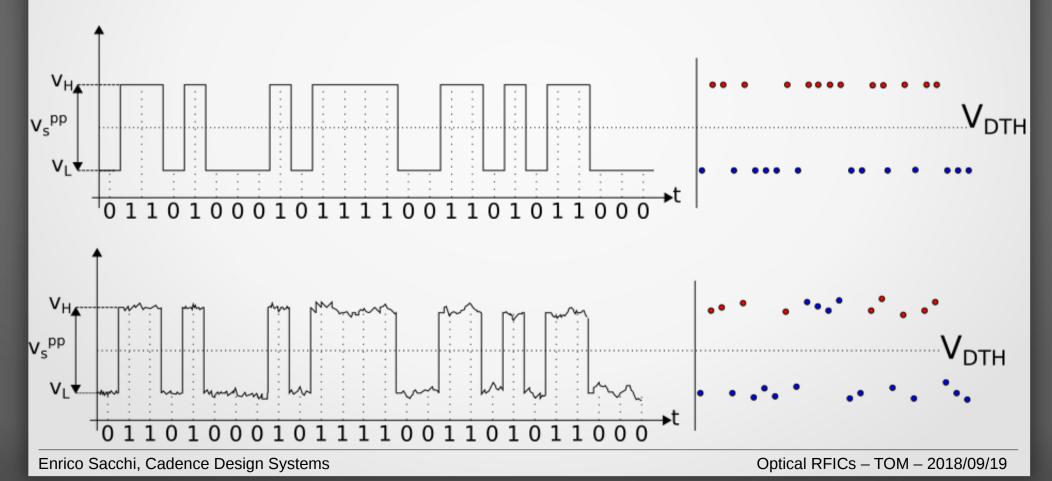
Bit-error rate (1/3)

- Let's simplify the scenario assuming a simple NRZ signal flowing through the system (without any ISI, jitter or other non-idealities). At the output of the linear channel we will have $v_0(t)$ given by:
 - A desired voltage signal $v_s(t)$ with a given peak-to-peak voltage v_s^{pp}
 - An unwanted rms noise voltage v_nrms (t), gaussian and signal independent



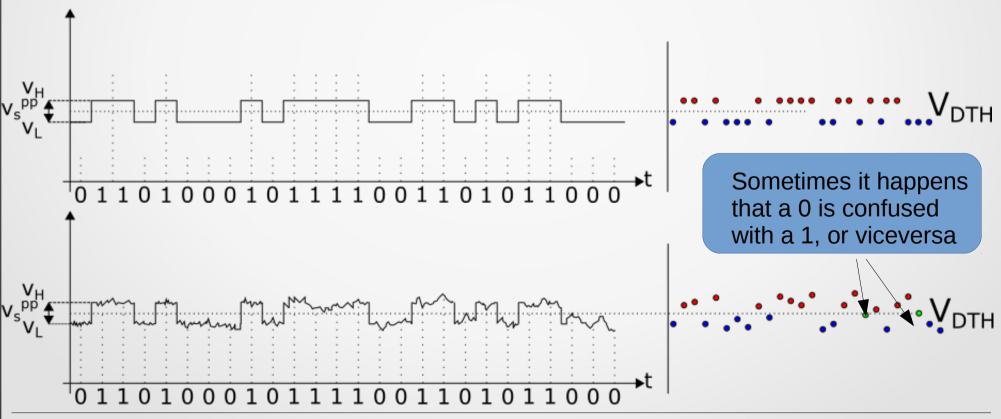
Bit-error rate (2/3)

• How the additive noise $v_n^{rms}(t)$ may corrupt the signal $v_s(t)$ thus causing an error at decision circuit level?

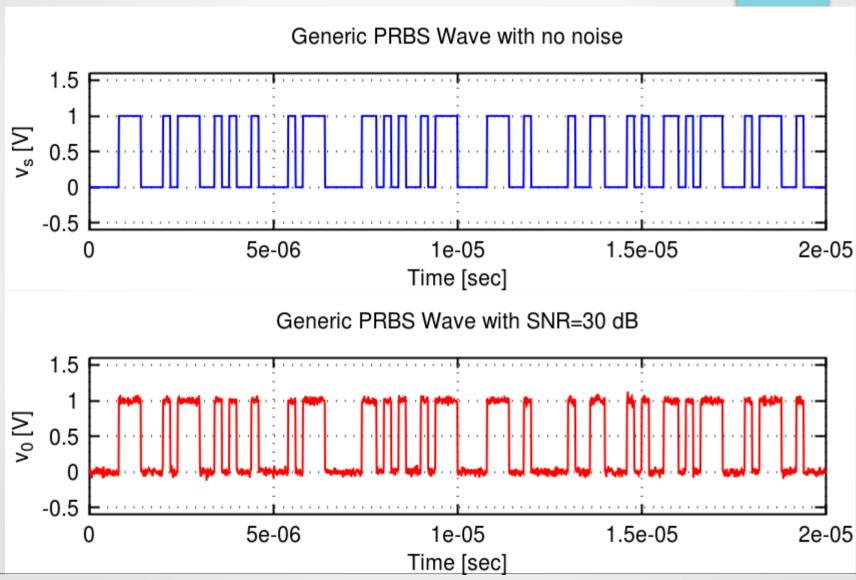


Bit-error rate (3/3)

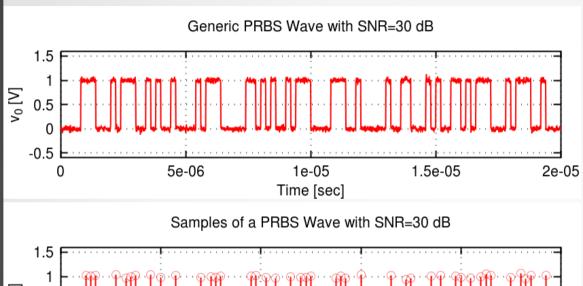
• Let's suppose that the same noise $v_n^{rms}(t)$ is added to a smaller signal vs(t), maybe because of an higher attenuation in front of the TIA or a lower efficiency of the photodiode

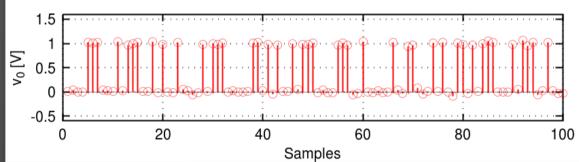


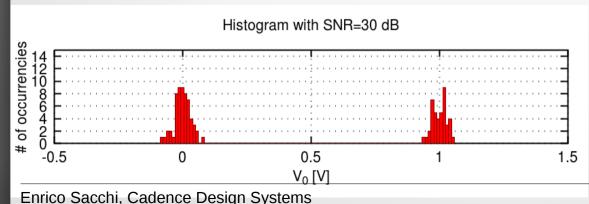
PRBS NRZ signal (100 bits)



100 bits PRBS with SNR=30 dB



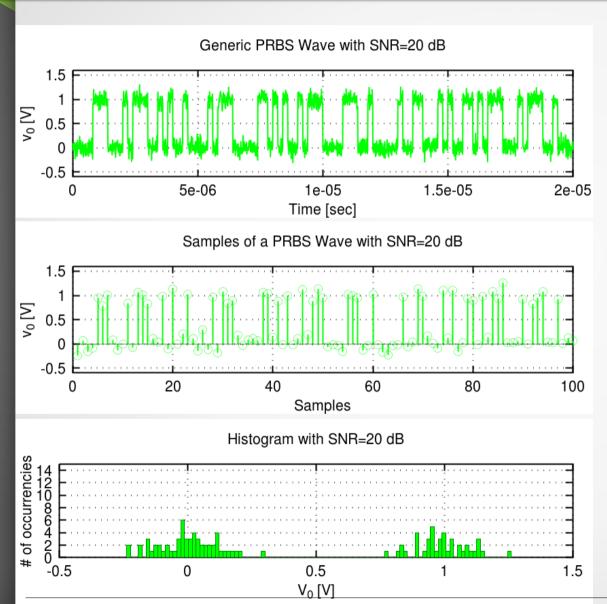




- A 30 dB NRZ signal seems to be close enough to the ideal one
- All the samples are around 1 when the signal is high and around 0 when the signal is low
- The histogram shows the "distribution" of the samples around the nominal values
- Being this a 100 sample example, we can conclude that:

BER << 10^-2

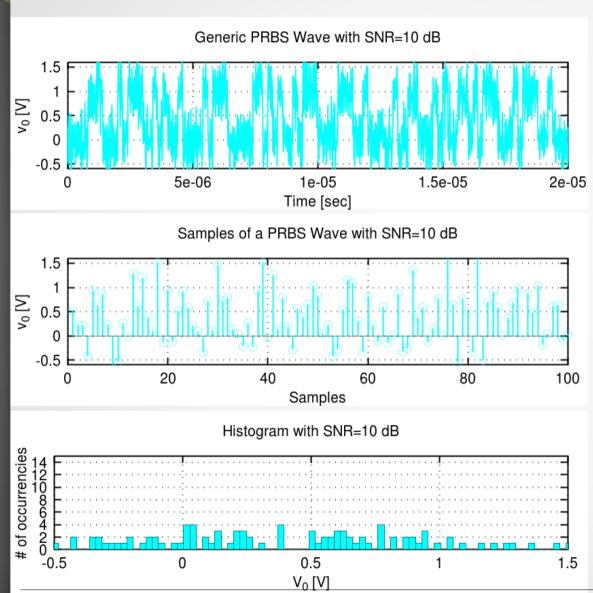
100 bits PRBS with SNR=20 dB



- A 20 dB SNR more significantly deteriorates the signal waveform
- The samples, when the signal is high and when the signal is low, are more "far away" from the nominal values 1 and 0
- The histogram shows that the "distribution" of the samples around the nominal values is a bit larger

BER < 10^{-2}

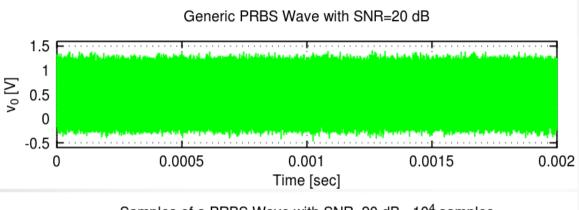
100 bits PRBS with SNR=10 dB

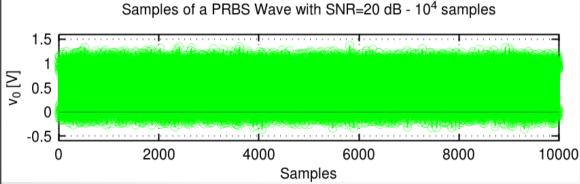


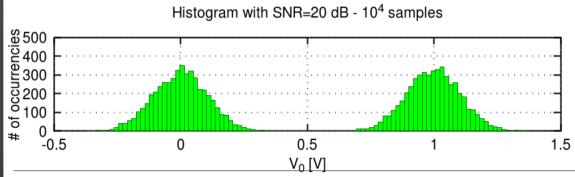
- An higher noise (SNR=10 dB) significantly corrupts the original signal
- Some sample when the signal is high risks to be interpreted as 0, and viceversa
- The histogram shows that the "distribution" of the samples is very broad

BER $\approx 10^{-2}$

10000 bits PRBS with SNR=20 dB





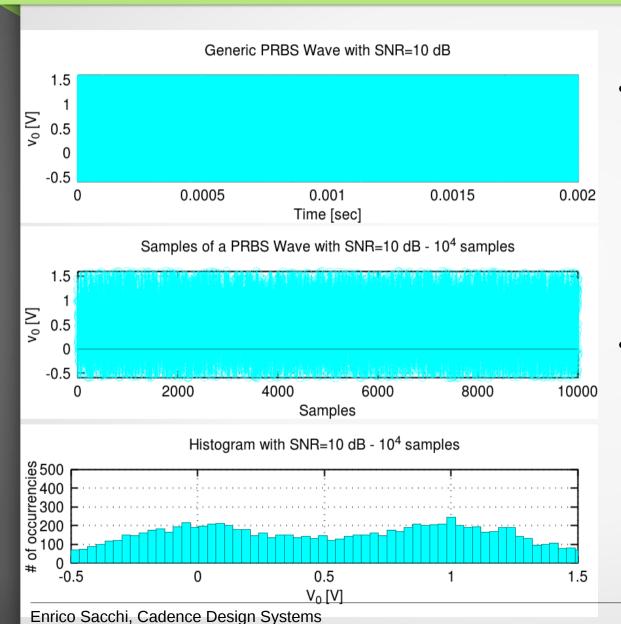


Enrico Sacchi, Cadence Design Systems

- Considering a longer bit sequence, it is possible to notice the stocastic nature of the noise
- While the SNR is always 20 dB, there are few samples that are significantly far away from the ideal 0 and
 1
- However, none of the samples is mis-interpreted, so we can conclude that the BER is lower than 10^-4

BER < 10^-4

10000 bits PRBS with SNR=10 dB

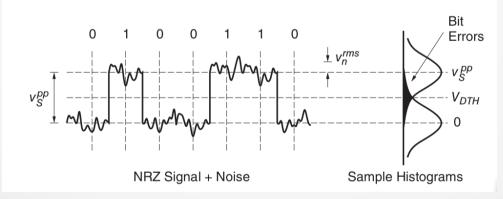


- raking 1000 samples of a signal with SNR=10 dB confirms that the BER is significantly higher than 10^-4, because some samples is erroneously interpreted by the decision circuit
- Histogram shows that there is no distinction between the distribution around 0 and around 1

BER >> 10^-4

BER definition (1/3)

- The decision circuit determines whether a bit is zero or one by comparing the sampled output voltage $v_0(t_{ns})$ with the decision threshold voltage v_{DTH} (usually set at the crossover point of the two distributions)
- BER is defined as the probability that a zero is misinterpreted as a one or a one is misinterpreted as a zero



$$BER = \frac{1}{2} \int_{V_{DTH}}^{\infty} \frac{1}{v_n^{rms}} Gauss\left(\frac{v_0}{v_n^{rms}}\right) dv_0 + \frac{1}{2} \int_{-\infty}^{-V_{DTH}} \frac{1}{v_n^{rms}} Gauss\left(\frac{v_0}{v_n^{rms}}\right) dv_0$$

BER definition (2/3)

Because of the symmetry, we can derive the following expression

-
$$BER = \int_{V_{DTH}}^{\infty} \frac{1}{v_n^{rms}} Gauss(\frac{v_0}{v_n^{rms}}) dv_0$$

 Gauss() is the normalized Gaussian distribution. If we then set, as it often happens, the decision threshold voltage to the midpoint

$$-V_{DTH} = \frac{v_s^{pp}}{2}$$

We then introduce the normalized variable

$$- x = \frac{v_0}{v_n^{rms}}$$

The following BER definition can be thus derived

BER definition (3/3)

•
$$BER = \int_{Q}^{\infty} Gauss(x) dx$$
 with

$$Q = \frac{v_s^{pp}}{2 v_n^{rms}}$$

Q is a parameter called "Personick" Q, that represents a measure of the ratio between signal and noise, but it is not exactly the SNR

Q	BER
0	0.5
3.090	10^-3
3.719	10^-4
4.753	10^-6
5.998	10^-9
7.034	10^-12
7.941	10^-15

FXAMPLF 1

- Signal swing at decision circuit: 650 mV pp
- RMS noise at decision circuit: 46 mV rms
- $Q=7.034 \rightarrow BER=10 \land -12$

FXAMPIF 2

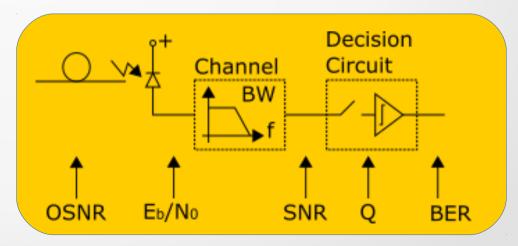
- Signal swing at decision circuit: 650 mV pp
- RMS noise at decision circuit: 41 mV rms
- $Q=7.034 \rightarrow BER=10 \land -15$

Signal to noise ratio (SNR)

- Signal to noise ratio (SNR) is defined as the mean-free average signal power divided by the average noise power
- Let's focus on an ideal NRZ signal, with v_s^{pp} swing, and with unequal noise on the zeros and the ones

$$SNR = \frac{(v_s^{pp})^2}{2(\overline{v}_{n,0}^2 + \overline{v}_{n,1}^2)}$$

$$\Rightarrow SNR = Q^2 \Rightarrow if \ v_{n,1}^{rms} = v_{n,0}^{rms}$$



$$\rightarrow SNR = Q^2/2 \rightarrow if \ v_{n,1}^{rms} \gg v_{n,0}^{rms}$$

$E_b/N_0 (1/2)$

- At the input of the receiver, before any filtering introduced by the "electronics", the noise can be considered as white, and its power spectral density is N₀
- Whatever is the signal amplitude, if we integrate N_0 over an infinite bandwidth we get SNR=0
- A more useful metric can be used to evaluate the quality of the signal at the input of the receiver: E_b/N_0
 - E_b: energy per bit, i.e., it is the average energy per information bit
 - N₀: one side noise spectral density

$E_b/N_0 (2/2)$

- The relation between E_b/N_0 and Q or SNR may be tricky to be calculated
- The simplest case is the DC balanced ideal NRZ signal; in this case

 The main difference between

$$E_b = \left(\frac{v_s^{pp}}{2}\right)^2 \cdot T'$$

- T' = T/r (duration of information bit)
- r = code rate

$$- N_0 = (v_n^{rms})^2 / BW_n$$

•
$$E_b/N_0 = Q^2 BW_n/r B = Q^2/2r$$

The main difference between $E_b/N0$ and Q or SNR is that E_b/N_0 takes the spectral efficiency of the modulation scheme into account

A more sophisticated, and efficient, modulation scheme, requires a lower E_b/N_0 at receiver input to get the same SNR at the output, if compared to simple NRZ

(Electrical) Sensitivity

- The electrical receiver sensitivty (i_{sens}pp) is defined as the minimum peak-to-peak signal current (i_spp) at the input of the receiver, necessary to achieve a specified BER (i_{sens}pp = i_spp@ BER)
- The sensitivity is related to the noise of the receiver

$$- i_{sens}^{pp} = \frac{2Qv_n^{rms}}{H_0}$$

- v_n^{rms} : rms noise voltage at the output of the receiver
- H_0 : low frequency value of receiver transfer function

$$- i_{sens}^{pp} = 2Q i_n^{rms} = Q (i_{n,0}^{rms} + i_{n,1}^{rms})$$

(Optical) Sensitivity

- The optical receiver sensitivity (\overline{P}_{sens}) is defined as the minimum optical power, averaged over time, \overline{P}_s , necessary to achieve a specified BER ($\overline{P}_{sens} = \overline{P}_s$ @ BER)
- $\bar{i}_s = i_s^{pp}/2$ In case of ideal NRZ

•
$$\bar{P}_s = i_s^{pp}/2R = \frac{Q(i_{n,0}^{rms} + i_{n,1}^{rms})}{2R}$$

Example:

-
$$I_n^{rms}$$
 = 1 µA, R=0.8 A/W, BER=10^-12 → Q=7.03

$$\overline{P}s = 8.79 \, \mu W = -20.6 \, dBm$$

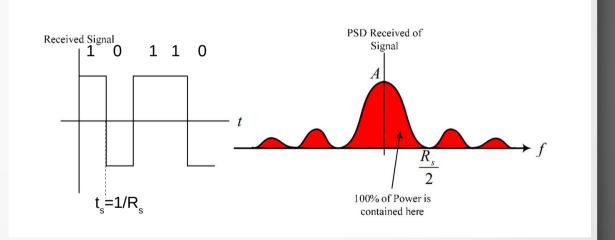
 The optical sensitivity is based on the average signal value, whereas the electrical sensitivity is based on the peak to peak signal value

Intersymbol interference (ISI)

- With any practical channel, the inevitable filtering effect will cause a spreading (or smearing out) of individual data symbols passing through the channel
- For consecutive symbols this spreading causes part of the symbol energy to overlap with neighboring symbols, causing intersymbol interference
- The result is that the received pulse corresponding to a particular symbol is affected by the previous symbol and subsequent symbols
- ISI is a kind of deterministic distortion, because it depends on the data pattern

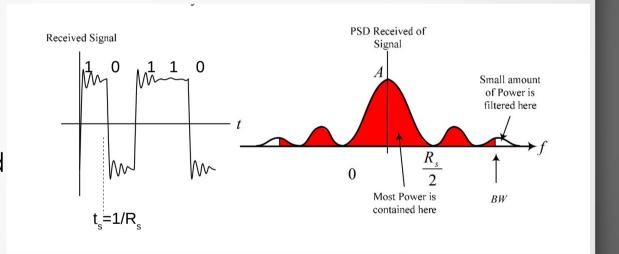
Channel with infinite bandwidth

- R_s: signal symbol rate
- The received signal will be exactly the same as the transmitted square wave
- No ISI at all
- The signal frequency bandwidth extends to infinite



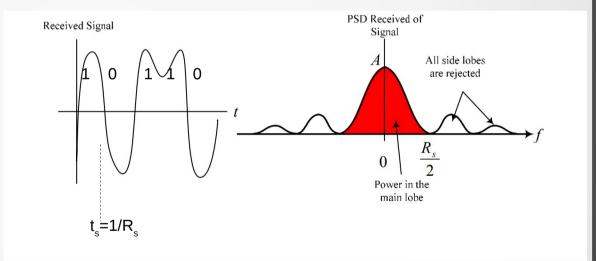
Wideband channel

- R_s: signal symbol rate
- The band of the channel is wide (> R_s/2) but not infinite
- A large amount of the signal power will pass, and a small amount of high frequencies will be filtered out
- The received data, in this case, experiences some ISI but they can be easily recovered



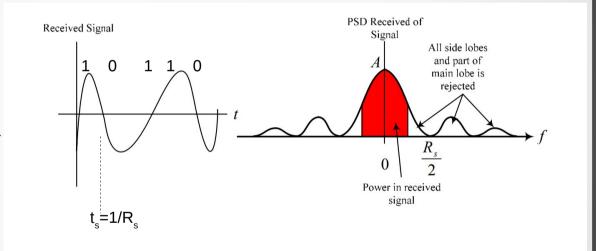
Channel bandwidth = R_s/2

- The first zero in PSD of transmitted data occurs at ½ the sample rate R_s
- The received signal in this situation experiences significant amount of ISI
- The data are still recoverable using some signal process algorithms



Channel bandwidth lower than R_s/2

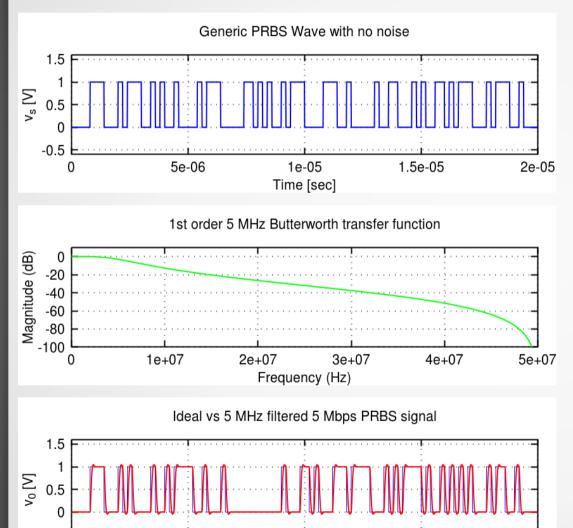
- When the channel bandwidth is significantly lower that R_s/2, the ISI is huge and loss of data will occur
- It is not possible to recover back the data completely, no matter what signal processing algorithms are used



Example: 5 Mbps / 5 MHz BW

1.5e-05

2e-05



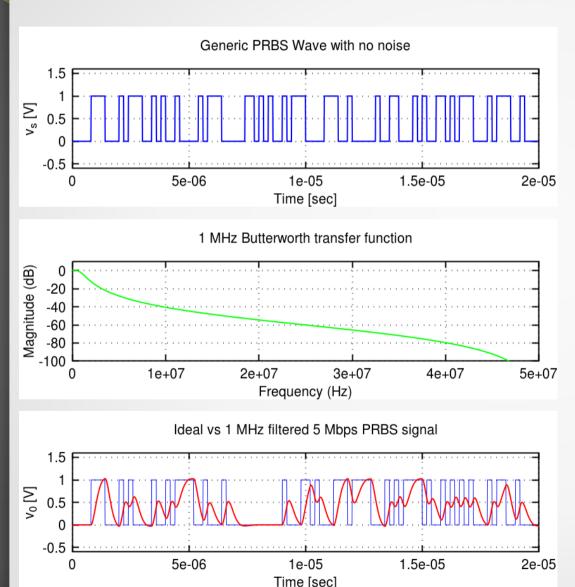
1e-05

Time [sec]

- Let's suppose to have an ideal NRZ PRBS signal, at 5 Mbps (f_s=5 MHz, T_s=200 n)
- The spectral components of such a waveform extends to infinite (because of the "vertical" transition slope)
- Let's suppose that such a signal passes through a 5 MHz BW channel
- The output signal (red curve) looks pretty similar to the input one

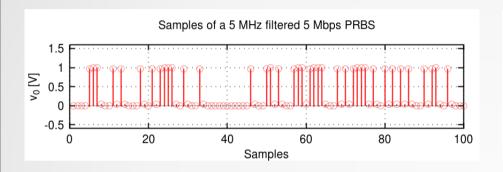
5e-06

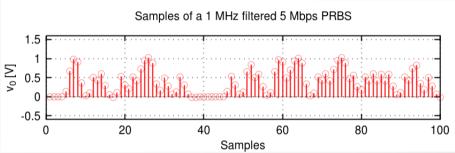
Example: 5 Mbps / 1 MHz BW

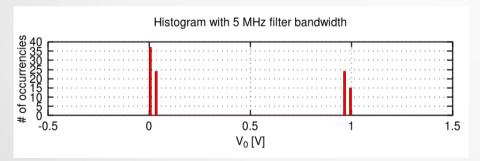


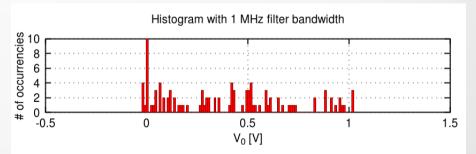
- Let's suppose to have the same ideal NRZ PRBS signal, at 5 Mbps ($f_s = 5$ MHz, $T_s = 200$ n)
- What happens if the channel bandwidth is significantly lower (1 MHz, in this example)?
- The high frequency components of the input signal are significantly filtered out, thus changing the shape vs time of the output waveform
- Is there any impact on the bit error rate?

Impact of ISI on bit error rate





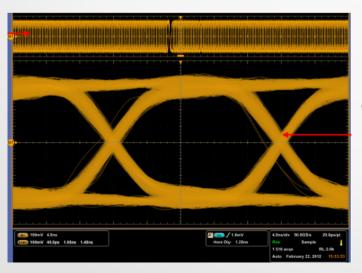




 ISI alone does not cause any bit error in the receiver as long as the "eye" has some opening left, and the decision threshold is located in that opening (deterministic effect)

Eye diagram (1/2)

- An "eye diagram" is a common indicator of the quality of signals in high speed digital transmissions
- An oscilloscope generates an eye diagram by overlaying sweeps of different segments of a long data stream driven by a master clock
- In an ideal world, eye diagrams would look like rectangular boxes. In reality, communications are imperfect, so the transitions do not line perfectly on top of each other, and an eye-shaped pattern results



Oscilloscope "eye diagram" example

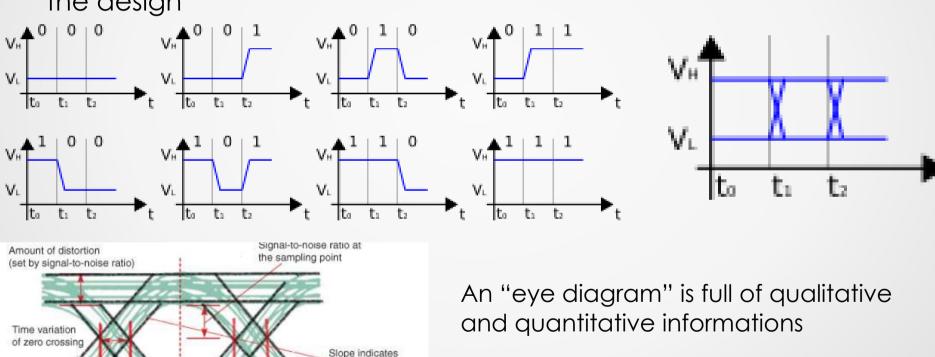
Eye diagram (2/2)

Best time to sample (decision point)

Most open part of eye = best signal-to-noise ratio

Measure of litter

 A properly constructed eye should contain every possible bit sequence from simple alternate 1's and 0's to isolated 1's after long runs of 0's, and all other patterns that may show up weaknesses in the design



sensitivity to timing error; the smaller, the better

Pulse shaping to control ISI

- To combat ISI, the pulses that we use to transmit data must have limited bandwidth, so that, when transmitted over limited bandwidth channels, the complete spectrum of these signals is retained, and no part is filtered out
- Unfortunately, limiting the bandwidth of the pulses causes their duration in time to be infinite: so each pulse extends over a very large number of bit periods
- This is not necessarily bad (if the pulse is designed properly)
- Nyquist criterium: each pulse is zero at the sampling time of other pulses

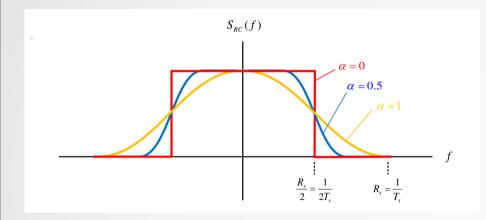
Raised cosine pulses

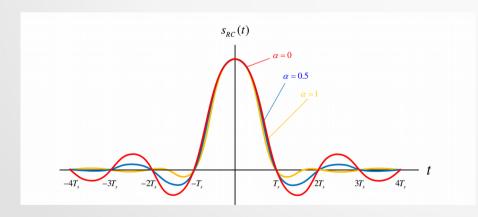
• The class of raised cosine pulses (including the sinc pulse as extreme case, α =0) respects the Nyquist criterium

$$s_{RC}(t) = \frac{\sin(\pi t T_s)}{\pi t} \frac{\cos(\frac{\pi \alpha t}{T_s})}{1 - (\frac{4 \alpha t}{2T_s})^2}$$

- α is a parameter that provides the trade-off between the bandwidth (which is limited) and tail length of the raised cosine function (how fast the pulse response becomes small)
- Normally the tail dies out after few bit periods

Raised cosine filter: pulse and spectrum





• The symbol rate (R_s) of the data that can be transmitted using a raised cosine pulse is related to α , and the bandwidth of the signal B, by the relation

$$R_s = \frac{1}{T_s} = \frac{B}{1 + \alpha}$$

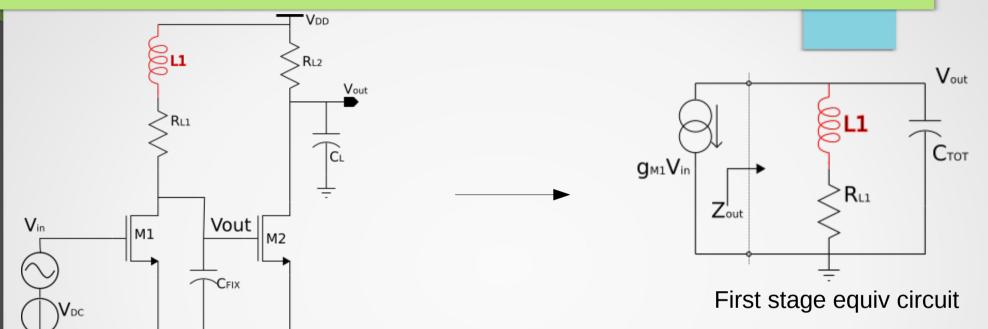
Outline

- (Short) Introduction to Optical Communications
- Broadband Techniques
- Optical RFICs
 - Transimpedance Amplifier (TIA)
 - Modulator Driver
- Conclusions

Broadband techniques

- Series and shunt peaking
- T-coil
- Neutralization
- Cherry-Hooper amplifier
- Capacitive degeneration
- Distributed amplifier

Shunt peaking (1/5)



$$A_{v} = \frac{V_{out}}{V_{in}} = g_{m1} \cdot Z_{out} = g_{m1} R_{L1} \cdot \frac{s(L_{1}/R_{L1}) + 1}{s^{2}L_{1}C_{TOT} + sR_{L1}C_{TOT} + 1}$$

- Inserting an inductance L1 in series with the resistive load R_{L1} , a zero in the transfer function is added
- The zero can be used to "cancel" the pole of the transfer function thus creating, within a band of frequencies, a flat-frequency response

Shunt peaking (2/5)

The transfer function can be rewritten as

$$A_{v} = g_{m1} R_{L1} \cdot \frac{1 + s \tau}{1 + s \tau m + s^{2} \tau^{2} m^{2}}$$

- where $\tau = L_{\scriptscriptstyle 1}/R_{\scriptscriptstyle L\,\scriptscriptstyle 1}$ and $m = R_{\scriptscriptstyle L\,\scriptscriptstyle 1}C_{\scriptscriptstyle TOT}/\tau$
- If L₁=0 the 3 dB bandwidth is defined as

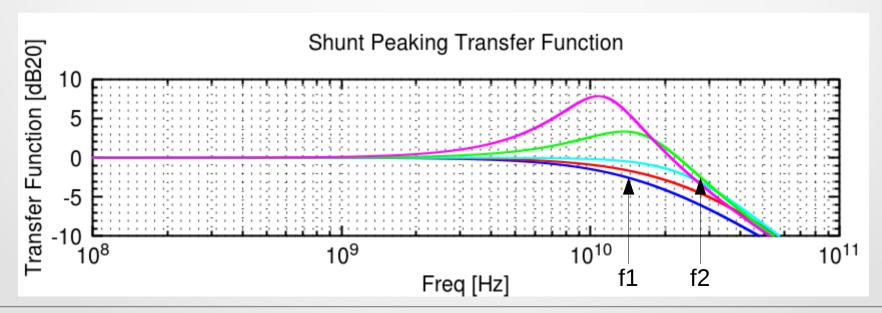
$$f_1 = 1/(2\pi R_{L1}C_{TOT})$$

 while, adding L₁, it is possible to demonstrate that the 3 dB bandwidth improvement is

$$\frac{f_2}{f_1} = \sqrt{(1+m-\frac{m^2}{2})+\sqrt{-(1+m-\frac{m^2}{2})^2+m^2}}$$

Shunt peaking (3/5)

- Once the bandwidth extension ratio is set, the value of L₁ is determined
- Example: $R_{L1} = 50 \Omega$, $C_{TOT} = 200f$, $g_{m1} = 20mS$
 - L_1 =0, L_1 =100 pH, L_1 =200pH, L_1 =500 pH, L_1 =1 nH



Shunt Peaking (4/5)

- Highest bandwidth extension (f2/f1=1.85) happens for m = 1.41, but we observe also a significant peaking (eye opening issue, in many cases)
- A maximally flat response is achieved setting m=2.41, but the bandwidth extension is limited to 1.72
- If phase response (group delay) is important, m has to be set to 3.1, but the corresponding bandwidth extension is "only" 1.6
- Usually the choice of the best "m", and thus of the best
 "L₁" value is set looking at the eye diagram

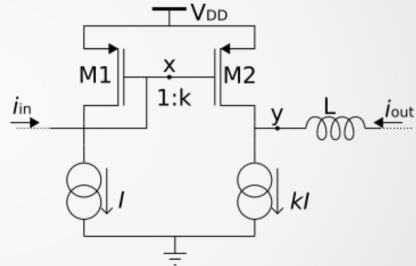
Shunt peaking (5/5)

 Shunt peaking can be applied also in current mode amplifiers

$$- C_x = C_{gs1} + C_{gs2} + C_{db1} + C_{gd2}''$$

$$- C_y = C_{gd2}' + C_{db2}$$

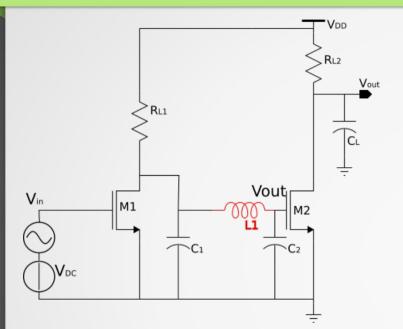
$$\frac{i_{out}(s)}{i_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right) \cdot \frac{1}{s \frac{C_x}{g_{m1}} + 1} \cdot \frac{\frac{1}{LC_y}}{s^2 + \frac{1}{LC_y}}$$



 The first part of the TF is the one of the basic current mirror, while the second part generates a "boost" in frequency, whose value depends on L

B.Sun, F.Yuan and A.Opal," *Inductive peaking in wideband CMOS current amplfiers*", 2004 IEEE International Symposium on Circuits and Systems, Vancouver, Canada

Series peaking



$$g_{M1}V_{in}$$
 Z_{out}
 R_{L1}
 C_1
 C_2
First stage equiv circuit

$$\tau = L_1 / R_{L1}$$

$$m = R_{L1} C_{TOT} / \tau$$

$$A_{v} = g_{m1} \cdot Z_{out} = g_{m1} R_{L1} \cdot \frac{1}{s^{2} L_{1} C_{TOT} + s R_{L1} C_{TOT} + 1}$$

- Lack of zero, in the transfer function, compared to shunt peaking
 - Less powerful than shunt peaking
 - Maximum bandwidth extension set to 1.41 with m=2

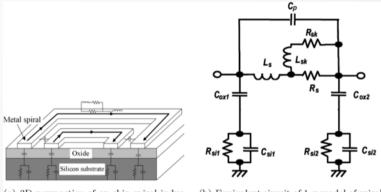
Series peaking with C₁

• If C_1 is not negligible, let's define $k_c = C_1/C_2$

k _c	Peaking [dB]	m	BW EXT
0	0	2	1.41
0.1	0	1.8	1.58
0.2	0	1.8	1.87
0.3	0	2.4	2.52
0.4	1	1.9	2.75
0.5	3.3	1.5	2.65

Integrated inductors

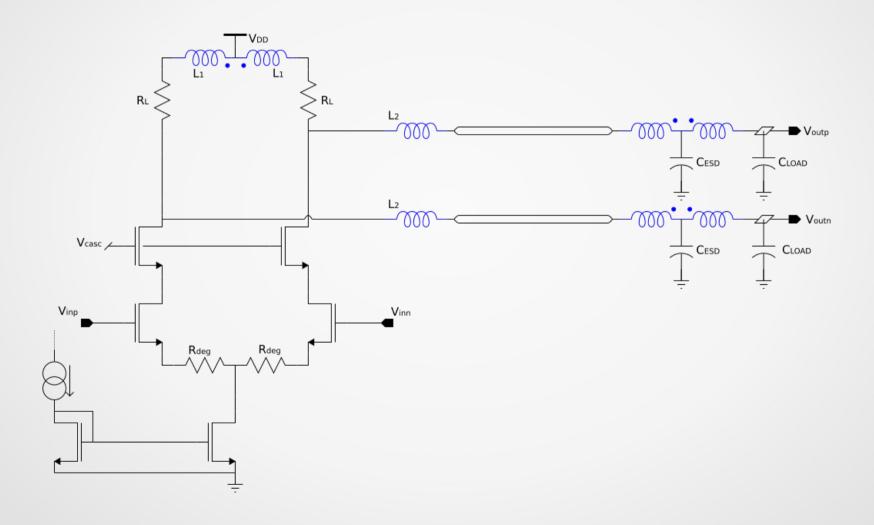
- Inductors implemented in CMOS and BiCMOS integrated circuits show a lot of non-idealities
 - Quality factor (metal series resistance, substrate losses)
 - Self-resonance frequency (substrate capacitance, fringing cap)
 - Electromagnetic coupling



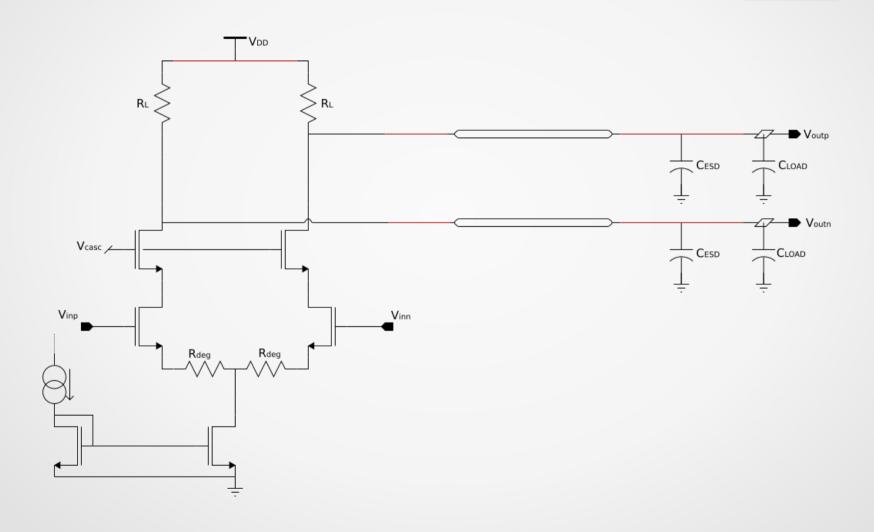
(a) 3D perspective of on-chip spiral induc- (b) Equivalent circuit of 1- π model of spiral tor [14]

- Usually not correctly modeled → need of accurate EM simulations
- What if we use shunt/series peaking with real life inductors?

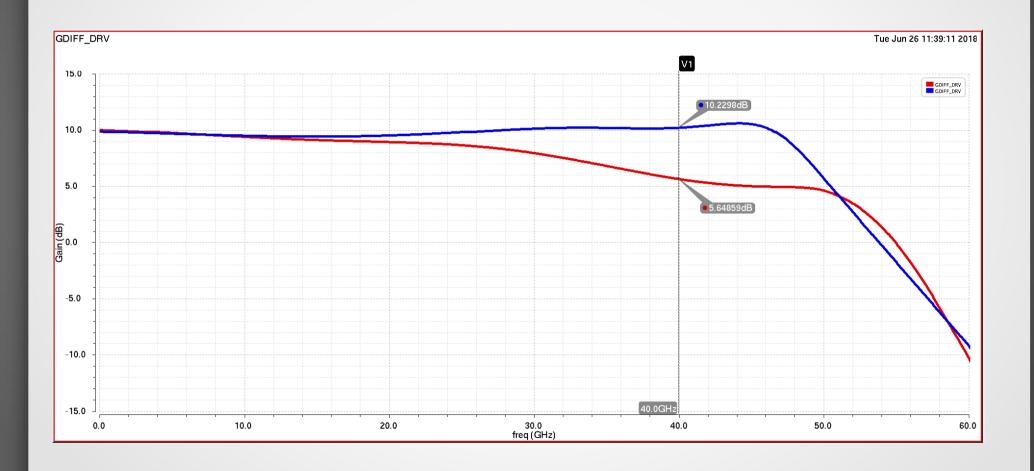
Buffer with shunt and series peaking



Buffer without shunt and series peaking

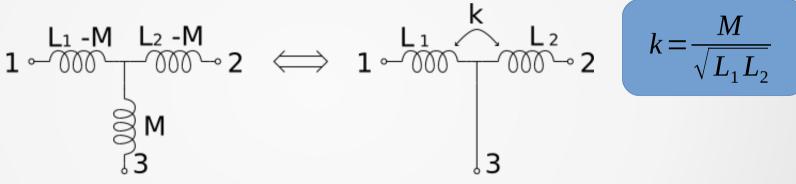


Gain vs frequency: comparison



T-coil (1/2)

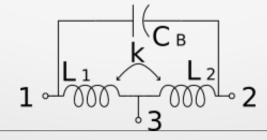
 A bridged T-coil is a circuit that extends the bandwidth by a greater factor than does inductive peaking



Impossible to be integrated (three not coupled spiral inductors)

Compatible with integration (two coupled spiral inductors: transformer?

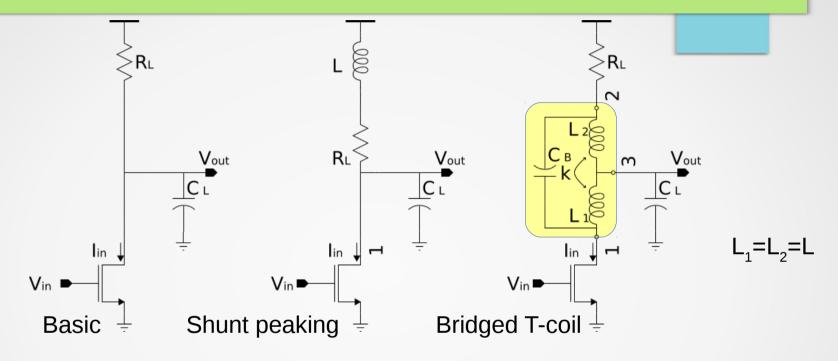
It consists of two mutually coupled inductors and a bridge cap



T-coil (2/2)

- With certain loads attached to this circuit, the impedance seen at node 1 or 2, and the transfer function from either of these nodes to node 3 present interesting properties
 - Amplifier bandwidth extension: in this case the signal current is injected in port 1, while the resistive load is connected to port 2, and the output capacitive load is connected to port 3
 - ESD protection: at the input and output pad of high speed circuits, ESD protection (from 250V up to 1kV for optical communications) is needed. However the parasitic cap associated with ESD structure (tens of fF) may limit circuit bandwidth and impact on return losses specifications

T-coil: bandwidth extension

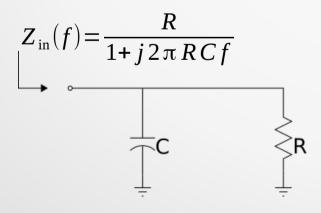


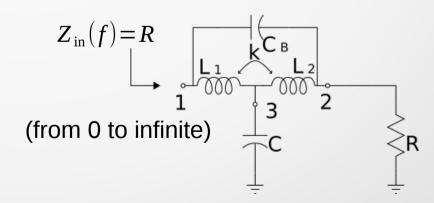
$$\frac{V_{\text{out}}(s) = -g_m R_L \frac{\omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \qquad \omega_n^2 = \frac{2}{(1-k)LC_L} \qquad \zeta = \frac{R_L C_L - (1-k)L/R_D}{\sqrt{2(1-k)LC_L}}$$

- The dumping factor ξ sets the bandwidth extension (ξ =0.7 \rightarrow 2.83), significantly wider than with shunt peaking
- Once ξ is decided, the other parameters L, k and C_B are derived

T-coil: constant impedance

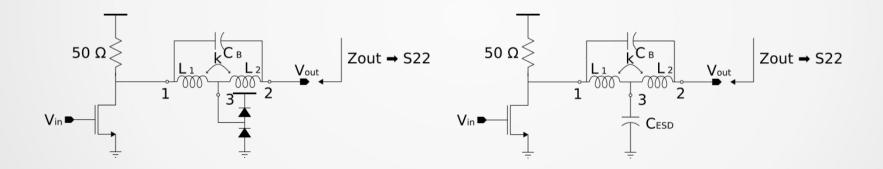
- The "black magic" behind a bridged T-coil allows its use also in another way, always useful for broadband applications
 - If opportunely connected and sized, the bridged T-coil can create a constant input (or output) impedance in the presence of an heavy load capacitance





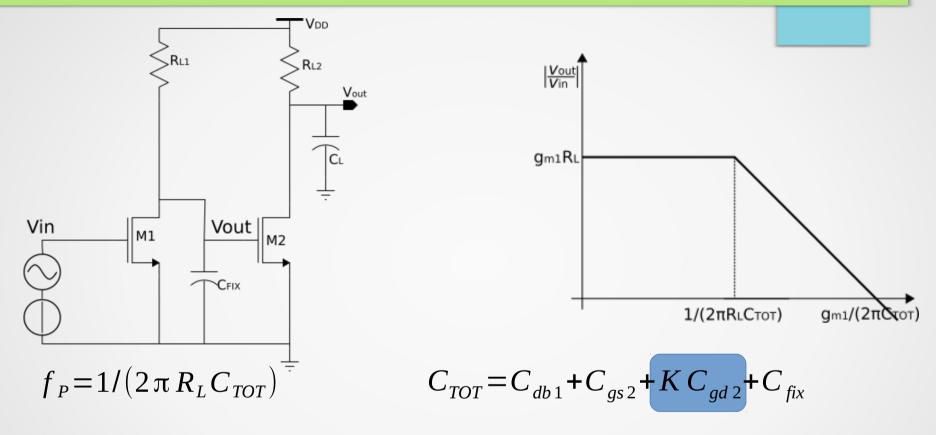
T-coil: ESD parasitics canceling

- For high speed wide-band circuits the possibility to cancel the effects of a parasitic cap is helpful
 - Example: return loss spec in presence of ESD parasitics



- T-coil inductance L₂ is not ESD protected (careful design)
- Additional cap at transistor drain or associated to the pad can't be canceled through T-coil

Amplifier bandwidth extension



- For a fixed DC gain and power consumption, the only way to increase the amplifier bandwidth is to reduce C_{TOT}
- Capacitance C_{gd2} is amplified by Miller effect

Miller effect on C_{GD}

• C_{gd} , with MOS in saturation region, is mainly overlap capacitance; it is not negligible compared to C_{gs} , but the ratio is technology dependent

$$Z_{\rm in} \approx \frac{1}{s(C_{gs} + C_{gd} \cdot (1 - A_{v}))} = \frac{1}{sC_{gs}(1 + C_{gd}/C_{gs} \cdot (1 + g_{m2}R_{L}))}$$

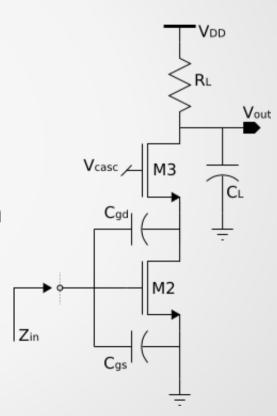
• If the gain $(g_{m2} R_L)$ is relatively high, the amplified C_{gd} dominates over C_{gs} also in the most recent technologies

Cascode

• The cascode device M_3 lowers the gain seen by $C_{\rm gd}$

$$A_{V} \approx g_{m2} \cdot \frac{1}{g_{gm3}}$$

- The impact of C_{gd} on bandwidth limitation is then reduced
- As a drawback, the added cascode lowers the achievable voltage swing at output node

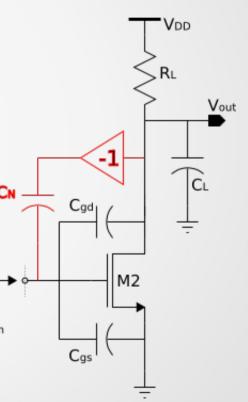


Neutralization (1/2)

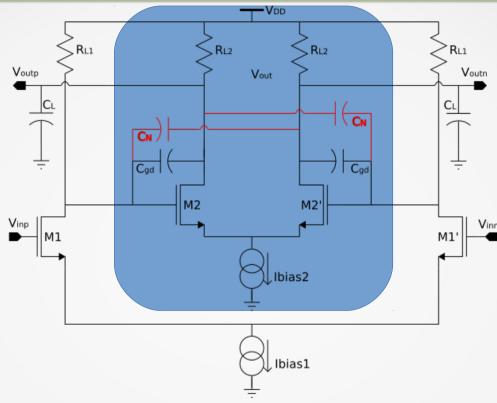
- C_{gd} impacts on bandwidth of the amplifier because a portion of the signal current flows into it
- Let's add a "neutralization" capacitance, driven by an ideal inverting stage (red)
- The current flowing into C_{gs} is now provided by C_N . No more impact of C_{ad} on input impedance C_N .

$$Z_{\rm in} \approx \frac{1}{s \, C_{gs}}$$

- Issues
 - How to implement the inverting amplifier?
 - Matching between C_N and C_{gd}



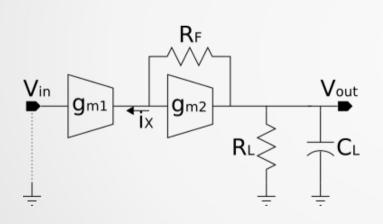
Neutralization (2/2)



- In differential implementation, the inverting buffer comes for free
- Matching issue C_N vs C_{gd}
 - If C_N too low, partial "cancellation of C_{gd}
 - If C_N too high, input impedance with inductive component (peaking)

Cherry-Hooper amplifier (1/3)

 The Cherry-Hooper topology was devised to allow the gain and bandwidth of an amplifier to be tuned independently of each other

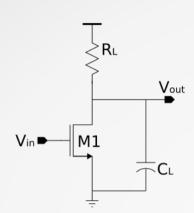


$$\frac{V_{\text{out}}(s) = (g_{m2}R_F - 1)(\frac{g_{m1}R_L}{1 + g_{m2}R_L}) \frac{1}{1 + \frac{sR_LC_L}{1 + g_{m2}R_L}}$$

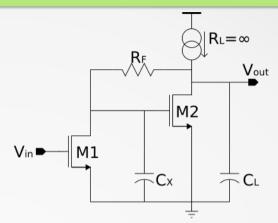
if
$$g_{m2}R_L$$
 and $g_{m2}R_F \gg 1 \rightarrow \frac{V_{\text{out}}}{V_{\text{in}}}(s) \approx \frac{g_{m1}R_F}{1 + \frac{sC_L}{g_{m2}}}$

• The gain only depends on the feedback resistor $R_{\scriptscriptstyle F}$ and $g_{\scriptscriptstyle m1}$, while the bandwidth only depends on $g_{\scriptscriptstyle m2}$ and the load capacitance $C_{\scriptscriptstyle L}$

Cherry-Hooper amplifier (2/3)







"Cherry-Hooper" amplifier

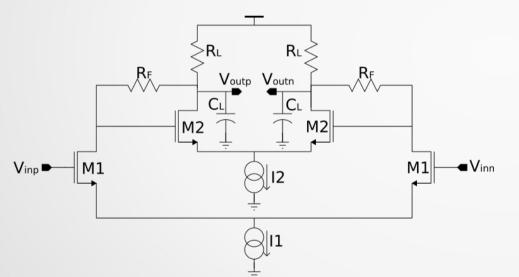
- In a conventional common source amplifier gain is proportional to R_{L1} , while bandwidth is inversely proportional to R_{L1} (trade-off)
- In "Cherry-Hooper" amplifier a feedback resistance R_F is used to sense the output voltage of the second stage and injecting a current back to the first stage

$$\frac{V_{\text{out}}}{V_{\text{in}}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}} = g_{m1}(R_F - \frac{1}{g_{m2}})$$

• If $R_F >> 1/g_{m2}$ the gain is similar to a common source stage having R_F as load resistor

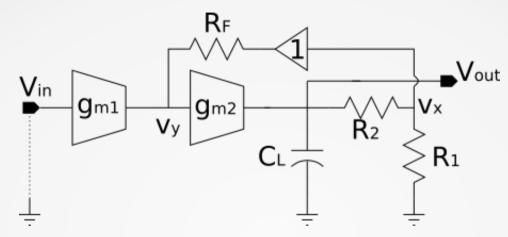
Cherry-Hooper amplifier (3/3)

- The key advantage of the Cherry-Hooper stage lies in the small-signal resistance seen at node X and Y (roughly equal to $1/g_{m2}$)
 - The associated poles move to high frequency



- Gain: R_F or g_{m1} must be increased
 - R_F or $g_{m1} \uparrow \rightarrow V_{G2} \downarrow$ (dynamic range)
- Bandwidth: C_L is not under control; $g_{m2} \uparrow \rightarrow$ out common mode
- The Cherry-Hooper design essentially moves the design trade-off from gain and bandwidth to gain/bandwidth and dynamic range

Modified Cherry-Hooper design (1/2)



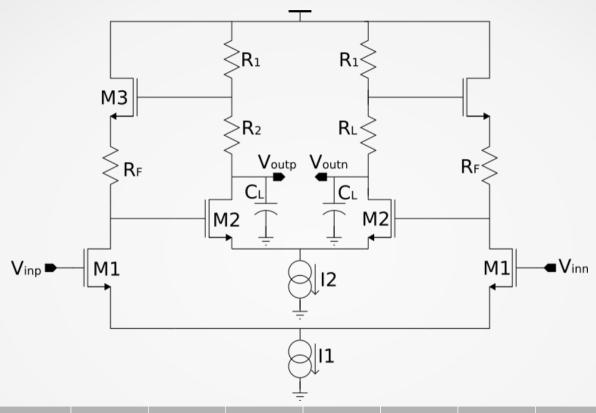
- A resistor divider (R1/R2) is added to the feedback path. Only a fraction of the output voltage is buffered back to the input
- This allows the designer to increase the gain of the amplifier without increasing $R_{\scriptscriptstyle F}$ or $g_{\scriptscriptstyle m1}$

$$H(s) \approx g_{m1} R_F (1 + \frac{R_2}{R_1}) (\frac{1}{1 + sC_L g_{m2} (1 + \frac{R_2}{R_1})})$$
 if $g_{m2} R_1 \gg 1$

gain =
$$g_{m1}R_F(1+\frac{R_2}{R_1})$$

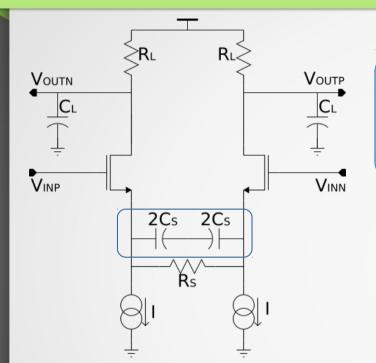
$$\omega_{3dB} = \frac{g_{m2}}{C_L \left(1 + \frac{R_2}{R_1}\right)}$$

Modified Cherry-Hooper design (2/2)



	R1 [Ω]	R2 [Ω]	RF [Ω]	I1 [mA]	I2 [mA]	g _{m1} [mS]	g _{m2} [mS]	C _L [fF]	Gain [dB]	F _{3dB} [GHz]	V _{CMOUT}
1	100	100	100	10m	10m	40	40	100	18	31	0.8
2	50	50	100	10m	20m	40	80	100	18	62	0.8

Capacitive degeneration (1/2)

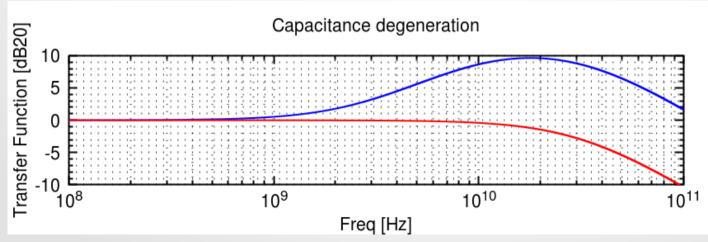


$$\frac{V_{\text{out}}(s) = \frac{g_{m1}R_L}{V_{\text{in}}} \frac{1 + \frac{s}{z_1}}{1 + \frac{g_{m1}R_s}{2} (1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

$$\omega_{z1} = \frac{1}{R_s C_s}$$

$$\omega_{z1} = \frac{1}{R_s C_s}$$
 $\omega_{p1} = \frac{1 + g_{m1} R_s / 2}{R_s C_s}$ $\omega_{p2} = \frac{1}{R_L C_L}$

$$\omega_{p2} = \frac{1}{R_L C_L}$$



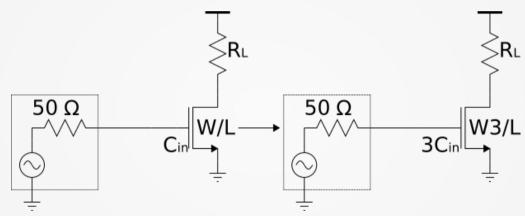
$$R_s$$
=150 Ω
 C_s =400 fF
 R_L =100 Ω
 C_L =50 fF
 g_{m1} =40 mS

Capacitive degeneration (2/2)

- Capacitive degeneration adds a zero ω_{z_1} and a pole $(\omega_{P1}>\omega_{Z1})$ to the transfer function, thus progressively increasing gain in the range $\omega_{Z1}<\omega<\omega_{P1}$
- Although bandwidth is effectively increased, it is not formally a bandwidth extension technique
 - Usually used as equalizing filter (for example in analog CTLE for SERDES), to compensate for frequency dependent losses in transmission media
 - Severe trade-off between gain and boosting:
 bandwidth is extended, but the boosting may be too much

Distributed amplifier (1/3)

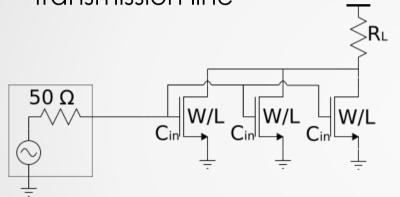
• For a fixed load resistance R_L , an amplifier achieves higher gain increasing the device size (and thus its g_m)

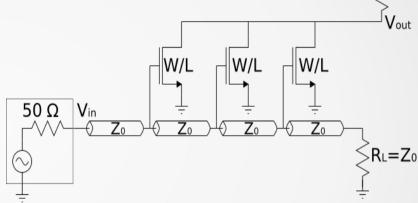


- Unfortunately, increased device size means higher input caps, thus lowering the bandwidth and getting an almost constant Gain x Bandwidth product
- However, transmission lines have ideally infinite bandwidth but can be modeled as LC networks

Distributed amplifier (2/3)

Lump input capacitance into LC network corresponding to a transmission line

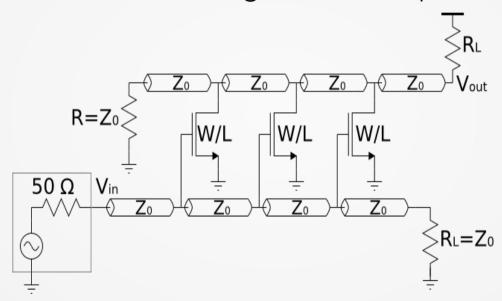




- Signal ideally sees a real impedance rather than an RC low pass
- Often implemented as lumped networks such as T-coils
- We can now trade delay (rather than bandwidth) for gain
- Issue: outputs are delayed from each other

Distributed amplifier (3/3)

 A solution is to delay the output as the inputs, using a similar transmission line, thus distributing also the output capacitance

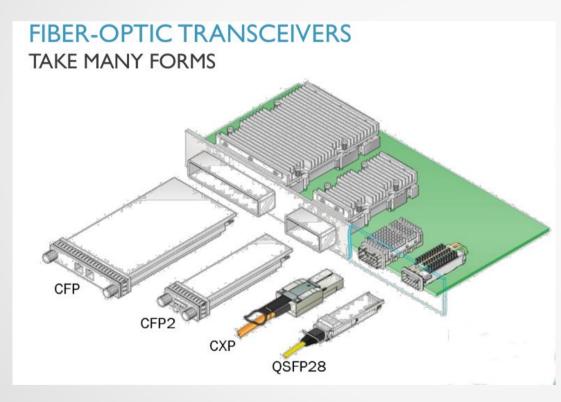


- High bandwidth but also high area occupation and poor noise performance
- Mainly used in GaAs MMIC, rarely in CMOS

Outline

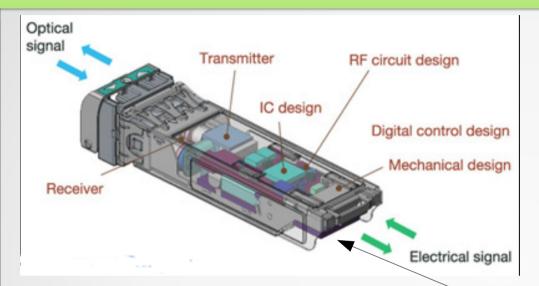
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Fiber optics transceivers



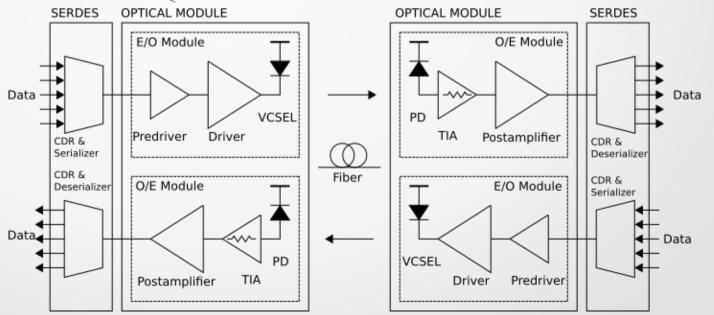
- Let's move more in the physical dimension
- An optical transceiver looks like a "connected box" with some standardized I/O, connecting the optical world with the electric one
 - CFP: Common Form Factor Pluggable
 - CXP: Common Transceiver (X) Pluggable
 - SFP: Small Form Factor Pluggable
 - QSFP: Quad Small Form Factor Pluggable

Optical modules



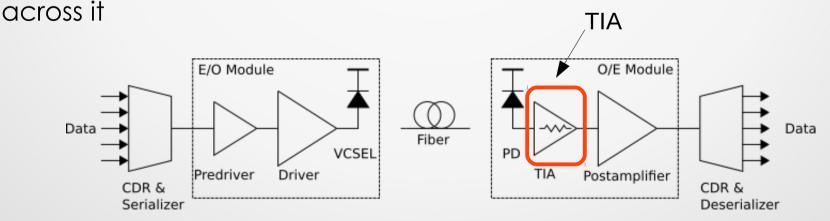
Example of optical module

Example of of highspeed communication system



TransImpedance Amplifier (1/2)

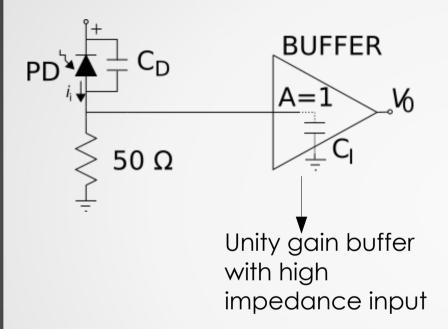
- The term TIA, in its wide sense, refers to any circuit that converts a current into a voltage;
- TIA must satisfy stringent requirements imposed by link budget (sensitivity, dynamic range, linearity) and speed considerations (bandwidth, ISI);
- Although it is often implemented using an amplifier, conceptually a simple resistance R_T, provides all the "transimpedance" characteristics, converting the flowing input current in voltage



TransImpedance Amplifier (2/2)

- A transimpedance amplifier converts an input current I_{in} (coming out from a photodiode) to an output voltage V_{out}.
- The circuit is characterized by a "transimpedance gain" R_T=dV_{out}/dl_{in}
- Since photodiodes generate a small current and most of the subsequent processing occurs in the voltage domain, the current must be converted to voltage
- Several types of transimpedance amplfiers have been proposed
 - Low impedance TIA
 - High impedance TIA
 - Shunt feedback TIA
 - Common base/gate TIA

Low impedance frontend (1/3)



- A 50 Ω load resistor converts PD current i_i into a proportional voltage (Ohm law)
- A unity gain buffer (with high input impedance, mainly capacitive) copies this voltage to the output V₀

- The most simple TIA you can imagine
 - Bandwidth limited by PD cap and buffer input cap
 - Noise from 50 Ω resistor (assuming ideal buffer)

$$V_0 = 50 \cdot i_i$$

At least at low freq

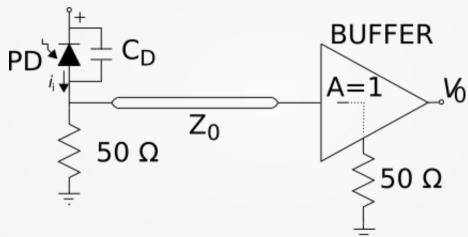
$$R_T = 50 \Omega$$

$$BW = 1/[2\pi 50(C_D + C_I)]$$

$$I_{n,res} = \sqrt{4 k T / 50} = 18 [pA / \sqrt{Hz}]$$

Low impedance frontend (2/3)

• A similar low impedance frontend may be realized also using a 50 Ω buffer (to make the connection between TIA and buffer more high frequency compliant)



• Because of the 50 Ω termination on both sides, we can use a standard Z_0 =50 Ω cable, without having to worry about reflections

$$V_0 = 25 i_i$$
 $R_T = 25 \Omega$ $BW = 1/[2\pi 25(C_D + C_I)]$

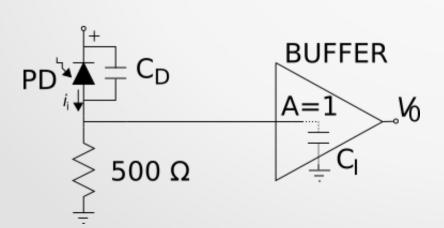
$$I_{n,res} = \sqrt{4 k T/50} = 18 [pA/\sqrt{Hz}]$$

Low impedance TIA (3/3)

- In general, although very simple, it is not good enough
 - Low transimpedance
 - Bad noise performance
- It can be useful only in application where circuit noise is not a primary concern
- Bandwidth is wide enough
- Example:
 - P_{OPT} =10 dBm, PD responsivity = 0.8 [W/A], R_T =25 Ω
 - V₀=400 mVpp, BW=42 GHz
 - Amplitude good enough for CDR, and bandwidth good for applications up to 50 Gbps, without stringent noise requirements

High Impedance TIA (1/2)

- Let's increase the load resistor R_T up to 500 Ω
 - Beneficial for transimpedance value (increased to 500 Ω)
 - Beneficial for noise performance
- Let's use same unity gain (noiseless) buffer as before
- Same PD capacitance C_D in parallel with C_I



$$R_T = 500 \Omega$$

$$BW = 1/[2\pi 500(C_D + C_I)]$$

$$I_{n,res} = \sqrt{4 k T / 500} = 5.8 [pA / \sqrt{Hz}]$$

High Impedance TIA (2/2)

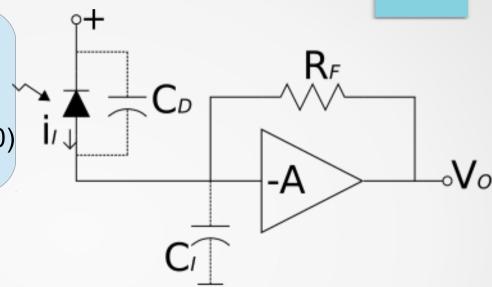
- Noise performance significantly improves, together with transimpedance value
- Bandwidth dramatically decreases, making the system not suitable for 10 Gbps application too, because of ISI
- Low input overload current
 - With relatively small TIA input currents (e.g. 2 mA), the input voltage swing may reach 1 V, thus causing input stage overload
 - Modulation of the reverse bias voltage of the photodetector

Noise and bandwidth tradeoff as a function of resistance value

Shunt Feedback TIA

Amplifier hypothesis

- Gain: A = infinite
- Output impedance: zero
- Input impedance: infinite (C,=0)
- BW: infinite



- All the current from the PD flows into R_F (with the exception of the current absorbed by PD capacitance itself)
- The input virtual ground keeps the reverse bias voltage of the PD constant (good overload behavior)

Less ideal shunt feedback TIA

- Let's make the circuit more realistic
 - Amplifier with finite gain A
 - Not negligible amplifier input capacitance C₁

$$C_T = C_D + C_I$$
 Total cap at TIA input

$$Z_{t}(s) = -R_{T} \frac{1}{(1+s/\omega_{p})}$$

$$R_{T} = \frac{A}{(A+1)} R_{F}$$

$$\omega_{p} = \frac{(A+1)}{(R_{F}C_{T})}$$

$$BW_{3dB} = \frac{\omega_{p}}{2\pi} = \frac{(A+1)}{2\pi R_{F}C_{T}}$$

$$C_{D}$$

$$C_{D}$$

$$C_{D}$$

$$C_{D}$$

$$C_{D}$$

$$C_{D}$$

Comments

- The transimpedance $R_{\scriptscriptstyle T}$ is approximately equal to the feedback resistor $R_{\scriptscriptstyle F}$, given a gain A that is much larger than unity
- The bandwidth is (A+1) times larger than that of an high impedance front-end with load resistor R_F and total capacitance C_T
- Additional benefit: the feedback reduces the TIA input impedance → higher input overload currents

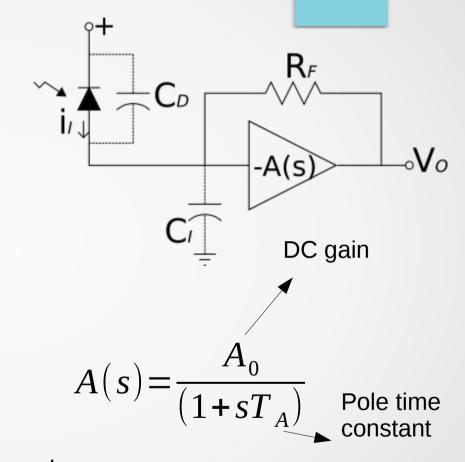
$$i_{ovl}^{pp} = \frac{(A+1)}{v_{I,ovl}^{pp}}$$

Finite amplifier bandwidth

- An amplifier cannot have infinite bandwidth, so let's approximate it to a more realistic single-pole amplifier
- The open-loop frequency response has 2 poles

$$- f_{I} = \frac{1}{(2\pi R_{F} C_{T})}$$

$$- f_{A} = \frac{1}{(2\pi T_{A})}$$



Low frequency pole

→ Stability, peaking

High frequency pole

Closed loop transimpedance

$$Z_{T}(s) = -R_{T} \frac{1}{(1+s/(\omega_{0}Q)+s^{2}/\omega_{0}^{2})}$$

$$R_T = \frac{A_0}{A_0 + 1} R_F$$

DC transimpedance

$$\omega_0 = \sqrt{\frac{A_0 + 1}{R_E C_T T_A}}$$

Angular frequency of the pole pair

$$Q = \frac{\sqrt{(A_0 + 1)R_F C_T T_A}}{R_F C_T + T_A}$$

Quality factor of the pole pair

The quality factor of the pole pair controls the peaking and the overshooting of the closed loop transfer function

Quality factor

- Q=1/sqrt(3)=0.577: Bessel response. It is characterized by a maximally flat group delay and it has not peaking in the amplitude response, with a very little overshooting
- Q=1/sqrt(2)=0.707: Butterworth response: maximally flat amplitude response with a small peaking in the group delay, and a bit more overshooting in the time domain
- To have a better dynamic stability (lower Q) demands a larger pole spacing f_A >> f_I

TIA Bandwidth

 Which is the bandwidth of a shunt feedback TIA based on a finite bandwidth amplifier, compared to one based on infinite bandwidth amplifier?

$$BW_{3dB} = \frac{\sqrt{2 A_0 (A_0 + 1)}}{2 \pi R_E C_T}$$

$$BW_{3dB} = \frac{A_0}{2\pi R_F C_T}$$

Single pole amp @ $f_A = \frac{1}{2 \pi R_E C_T}$

Infinite bandwidth amp

 TIA based on single pole amplifier shows a 3dB bandwidth higher than TIA based on infinite bandwidth amplifier (amazing result!!!)

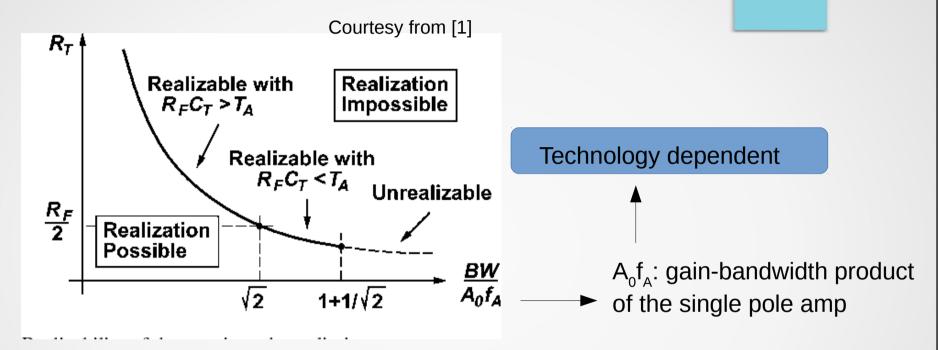
Transimpedance limit (1/2)

- Shunt-feedback TIA are usually designed to be "free" of amplitude peaking (Q<0.707)
- It can be demonstrated that in such a case the 3dB bandwidth of the TIA cannot be higher than $\omega_0/2\pi$

$$BW_{3dB} \le \frac{1}{2\pi} \sqrt{\frac{A_0 + 1}{R_F C_T T_A}} \longrightarrow R_T \le \frac{A_0 f_A}{2\pi C_T BW_{3dB}^2}$$

- There is a trade-off between the achievable transimpedance, and the TIA bandwidth!!
- For a given BW, there is a superior limit to the achievable transimpedance value

Transimpedance limit (2/2)



$$A_0 f_A \approx \frac{g_m}{2\pi C_L} = f_T \frac{C_I}{C_L}$$
 C: load cap of the transistor inside the amp C: amp input cap under shorted output cond.

 For a given technology (fixed A₀f_A) and a given photodector (fixed C_T) the attainable transimpedance drops with the square of TIA BW

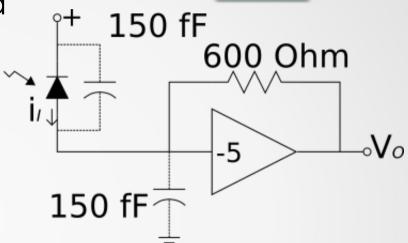
Example: 10 Gbps TIA (1/2)

Let's start with the following data

$$-A_0 = -5$$

$$- C_D = C_1 = 150 \text{ fF}$$

$$-R_F=600 \Omega$$



• A_0 and C_D are set by the technology used, while R_F is a first guess to achieve R_T high enough

$$R_T = \frac{5}{[5+1]} 600 \Omega = 500 \Omega \longrightarrow BW_{3dB} = \frac{\sqrt{2} A_0 (A_0 + 1)}{2\pi R_F C_T} = 6.85 GHz$$

Such a bandwidth is good enough for a 10 Gbps TIA (2/3 of baud rate)

Example: 10 Gbps TIA (2/2)

- Let's derive other TIA characteristics:
 - Amp pole frequency: $f_A = \frac{2A_0}{2\pi R_F C_T} = 8.84 \, GHz$
 - Amp Gain BW product: $A_0 f_A = 44.2 GHz$
 - Input impedance: $R_I = \frac{R_F}{A_0 + 1} = 100 \Omega$
 - Input ref current density*: $I_{n,TIA} = \frac{4 kT}{R_F} = 5.25 pA/\sqrt{Hz}$
- The low input impedance, for a fixed maximum permissible input voltage swing, allows for an higher input overload current
- * Please note that in the noise calculation, the amp noise has been neglected

A comparison

		Shunt-FB	Low-Z	High-Z
Transimpedance $[\Omega]$		500	50	500
3 dB Bandwidth [GHZ]	BW _{3dB}	6.85	11	1.1
Overload current [mA]	pp ovl	2	4	0.4
Noise current [pA/sqrt(Hz)]	I n,TIA	5.25	18	5.8

- Overload current has been evaluated assuming maximum overload voltage at input of 0.2 V
- Compared to Low-Z and High-Z TIA, the shunt feedback topology provides performance good enough for a low noise 10 Gbps TIA, while High-Z TIA shows BW limitation, and Low-Z TiA is too noisy

Example (MOS TIA)

	Symbol	10 Gbps	40Gbps
Gain-Bandwidth	$A_0 f_A$	44 GHz	177 GHz
PD capacitance	C_{D}	0.15 pF	75 fF
Amp. DC gain	A ₀	14 dB	14 dB
Amp. 3dB BW	f _A	8.8 GHz	35.4 GHz
Amp. Input Cap	C _I	0.15 pF	75 fF
Feedback Resistor	R_{F}	600 Ω	300 Ω
Transimpedance	R_{T}	500 Ω	250 Ω
Input Impedance	R_{I}	100 Ω	50 Ω
TIA 3dB BW	BW _{3dB}	6.85 GHz	27.4 GHz

Nonzero Amp. Output Impedance



$$Z_{T}(s) = -R_{T} \frac{1}{1 + s/\omega_{0} Q + s^{2}/\omega_{0}^{2}}$$

$$\begin{split} R_{T} &= \frac{A_{0}' R_{F} - R_{L}}{A_{0}' + 1} \qquad \omega_{0} = \sqrt{\frac{A_{0}' + 1}{R_{F} C_{T} T_{A}'}} \\ Q &= \frac{\sqrt{(A_{0}' + 1) R_{F} C_{T} T_{A}'}}{(R_{F} + R_{L}) C_{T} + T_{A}'} \end{split}$$

Please note that connecting the feedback resistor RF to the output alters both the gain and the time constant

 $A_0' = g_m R_L$ Unloaded Amp Gain $T_A' = R_L C_L$ Unloaded Amp Time Constant

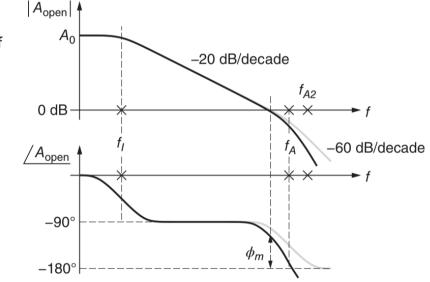
Comments

- The transimpedance expression has two poles and no zeros as it happens when the amp output impedance is zero
- The DC transimpedance (transresistance) is reduced by the factor $1-R_L/(A_0{'}R_F)$
- The pole frequency ω_0 remains unchanged
- The Q factor is reduced by the factor $R_F/(R_F + R_L)$
- The effect of the finite output impedance becomes negligible if we have $R_L\!\ll\!R_F$

Amp with non dominant poles

- An actual amplifier shows additional poles:
 - Cascode transistors
 - Level shifters
 - Broadband techniques
- 3 poles open loop freq resp.

$$f_I = 1/(2\pi R_F C_T)$$



- $f_A = 1/(2\pi T_A)$: amp dominant pole
- $f_{A2} = 1/(2 \pi T_{A2})$

Comments

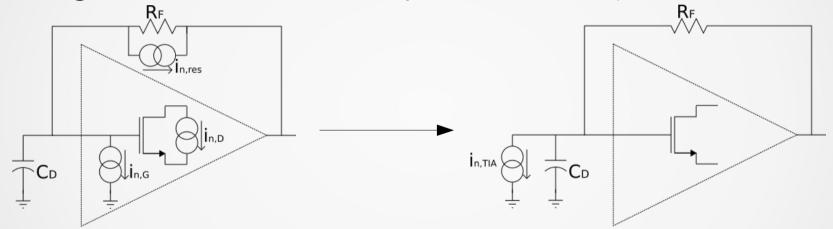
 The new non-dominant pole adds phase shift at the unity-gain freq: phase margin reduction

$$\Delta \phi_m \approx \tan^{-1} \left(\frac{A_0 T_{A2}}{R_F C_T} \right)$$

- To compensate for such degradation
 - The amp dominant pole has to be placed at higher frequency ($f_A > \frac{2A_0}{2\pi R_E C_T}$)
 - A capacitor C_F has to be added in parallel to feedback resistance R_F

Noise Analysis

 Till now we have always assumed the amp as noiseless, taking in consideration only noise from R_F



- Thermal noise from feedback resistor R_F
- Gate shot noise from TIA transistor
- Channel Noise and Induced Gate Noise from TIA transistor

Feedback Resistor Noise

• The noise current of the feedback resistor R_F is white and given by the well-known thermal noise equation

$$I_{n,res}^2(f) = \frac{4kT}{R_F}$$

- This noise contributes directly to the input-referred TIA noise because $i_{n,res}$ has the same effect on TIA output as $i_{n,TIA}$
- Once the desired transconductance is set (R_T ≈R_F), we cannot avoid this noise contribution, as higher as the transconductance is small

Gate Shot Noise

- Usually a MOS transistor exhibits a negligible gate current (and this is a significant difference with BJT)
- However in nanoscale technologies gate leakage increases rapidly [6]
- Metal semiconductor FETs (MESFETs) and heterostructure FETs (HFETs) can have gate currents up to 1 µA

$$I_{n,G}^2 = 2qI_G$$

Transistor Noise (1/2)

Thermal noise: caused by thermal fluctuations in the FET channel

$$I_{n, chan}^2 = 4kT \gamma g_{d0}$$

- k: Boltzmann constant
- g_{d0} :drain-source conductance at v_{ds} =0 V
- $g_{d0} \approx g_m + g_{mb} + g_0$

g_{mb}: substrate conductance

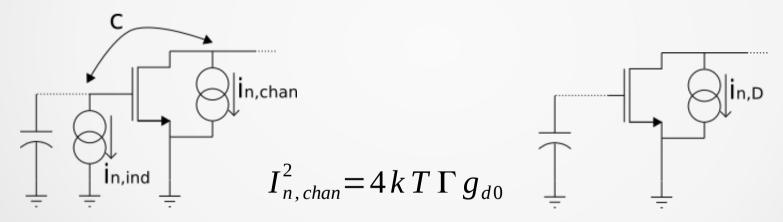
g₀: output transconductance

 Induced gate noise: caused by the capacitive coupling between the channel and the gate

$$I_{n,ind}^2 = 4 k T \delta \frac{2 \pi f C_{gs}^2}{5 g_{d0}}$$

Transistor noise (2/2)

- If the source impedance is capacitive, the induced gate noise produces a white gate noise voltage
- FET model with a single white drain noise generator I_{n,D}

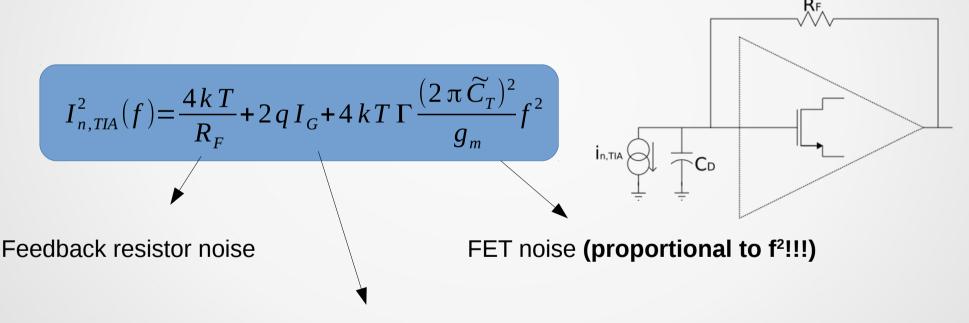


$$\Gamma = \frac{\gamma g_{d0}}{g_m} + (induced \ gate \ noise) \rightarrow Ogawa' noise factor$$

• $\Gamma \approx 2$ for long channel MOS devices

Input Referred Drain Noise

 Let's now calculate the input referred noise current PSD of the TIA based on MOS input stage [1]

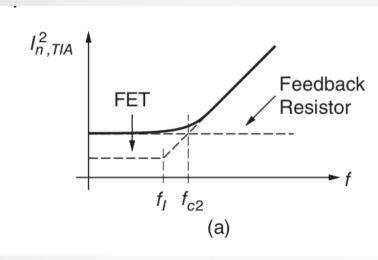


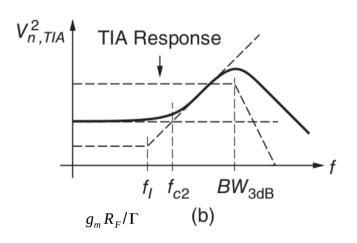
Gate shot noise (often negligible)

Input and output noise

Input noise current

Output noise voltage

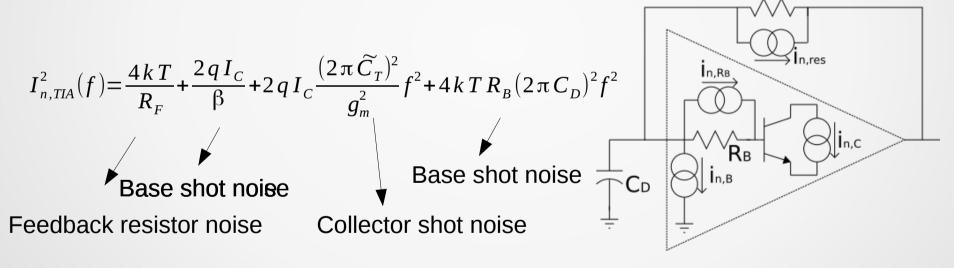




- The FET noise starts out below the feedback resistor noise (by a factor $g_m R_F/\Gamma$) and then begins to rise at the frequency $f_I = 1/2\pi R_F \widetilde{C}_T$
- The noise corner of the overall input-referred noise is at a frequency f_{c2} slightly higher than f₁
- For Butterworth transfer function, the 3 dB bandwidth is often higher than $f_{C2} \longrightarrow V_{n,TIA}$ may have an hump

Noise in BJT shunt feedback TIA

• In BJT implementation, a shunt feedback TIA shows also not negligible base shot noise ($I_{n,B}$) and thermal noise because of its base resistance [1]



 Regardless of weather the TIA has a FET or BJT frontend, the input referred noise current PSD is composed of white-noise terms and f² noise terms

Input-referred RMS noise current

 TIA sensitivity is set by the input-referred RMS noise current, while, till now, we just derived the input-referred noise current Power Spectral Density (PSD)

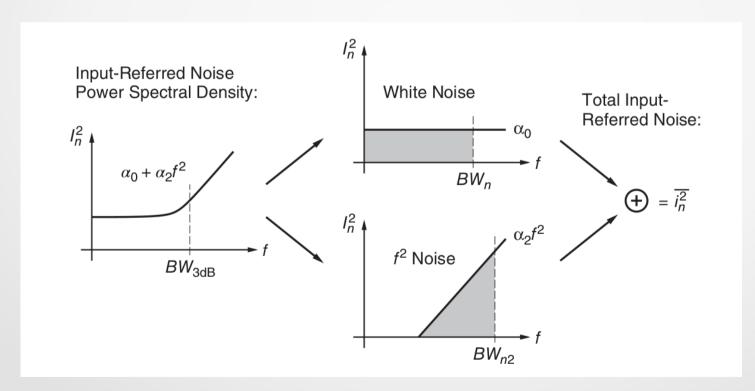
$$i_{n,TIA}^{rms} = \frac{1}{R_T} \sqrt{\int_0^\infty |Z_T(f)|^2 |I_{n,TIA}^2(f)|^2} df$$

 While the integral can be tricky to be solved by hands, input-referred RMS noise can be expressed in a different way

$$\overline{i_{n,TIA}^2} = \alpha_0 BW_n + \frac{\alpha_2}{3} BW_{n2}^3$$

Noise Bandwidth (1/2)

 BW_n and BW_{n,2} are called noise bandwidth, a quantity that depends only on the receiver's frequency response |H(f)| and the decision circuit bandwidths BW_d



Courtesy from [1]

Noise Bandwidth (2/2)

- Bw_n: noise bandwidth of the TIA for white noise
- Bw_{n2}: noise bandwidth of the TIA for f² noise
- For the shunt feedback TIA based on a single pole amplifier with infinite input and zero output impedance we get [1]:

$$BW_{n} = \frac{A_{0} + 1}{4(R_{F}C_{T} + T_{A})}$$

$$BW_{n2}^{3} = \frac{3(A_{0} + 1)^{2}}{16\pi^{2}(R_{F}C_{T} + T_{A})R_{F}C_{T}T_{A}}$$

$$i_{n,TIA}^{rms} \approx \sqrt{\left(\frac{4kT}{R_F} + 2qI_G\right)BW_n + \frac{1}{3}\left(4kT\Gamma\frac{(2\pi\widetilde{C}_T)^2}{g_m}\right)BW_{n2}^3}$$

for MOS TIA

Example (MOS TIA)

	Symbol	10 Gbps	40Gbps
Transition frequency	f _T	79.5 GHz	318 GHz
Ogawa Noise Factor	Г	2	2
Gate current	l _G	0	0
Transconductance	g_{m}	50 mS	100 mS
Amp. Input Cap	C _I	0.15 pF	75 fF
TIA 3dB Bandwidth	BW _{3dB}	6.85 GHz	27.4 GHz
Noise BW - white	BW _n	7.58 GHz	30.3 GHz
Noise BW - f ²	Bw _{n2}	10.22 GHz	40.9 GHz
Input rms noise curr	rms n,TIA	889 nA	2.51 μΑ
Average I _{n,TIA} rms	avg n,TIA	10.2 pA/sqrt(Hz)	14.4 pA/sqrt(Hz)

Noise Optimization (1/4)

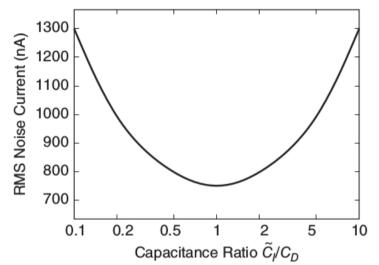
- Which is the best way to optimize MOS TIA noise performance?
 - Using parametric simulations: practical, but not useful to understand
 - Looking at noise equations, and understanding how to reduce as much as possible noise contributions

$$i_{n,TIA}^{2} \approx \frac{4 kT}{R_{F}} BW_{n} + 2 qI_{G} BW_{n} + 4 kT \Gamma \frac{\left[2\pi \left(C_{D} + \widetilde{C}_{i}\right)\right]^{2}}{3 g_{m}} BW_{n2}^{3}$$
Low gate leakage: $I_{G} < 2 V_{T}/R_{F}$

 $R_{\rm F}$ as high as possible: to be allowed to use high $R_{\rm F}$, considering the TIA limit, an high $f_{\rm T}$ helps

Noise Optimization (2/4)

$$4kT\Gamma \frac{[2\pi(C_D + \widetilde{C}_i)]^2}{3g_m}BW_{n2}^3$$



- This term increases with C_D + C_i
 - Reduction of photodiode, ESD, pad, input parasitic caps (C_D)
 - It is not obvious that reduction of C_i ($C_{gs} + G_{gd}$) is helpful because, for a fixed f_T , this term is proportional to g_m too
 - f_T as high as possible is helpful in term of noise performance
 - It is possible to demonstrate that $\widetilde{C}_i = C_D$ minimizes the 3rd term

Noise Optimization (3/4)

Let us add some additional constraint

$$f_I \approx 1/[2\pi R_F(C_D + \widetilde{C}_I)]$$
 Fixed open—loop input pole $f_A = 1/[2\pi T_A]$ Fixed open—loop output pole A_0 Fixed DC gain

- Fixed
 A₀f_A
 BW_{3dB}
 Q
- If C₁ increase (increasing FET width), R_F has to be decreased accordingly
- g_m increases too, thus R_L has to decrease, and C_L has to increase to keep f_A constant
- The optimum becomes $\widetilde{C}_I = \psi C_D$ with $\psi \approx \sqrt{\frac{\Gamma A_0 f_A}{\Gamma A_0 f_A + f_T}}$
- The optimum input cap is smaller than C_D

Noise Optimization (4/4)

 After this optimization, the input referred noise current becomes [1]

$$i_{n,TIA}^{rms} = BW_{3dB}\pi \left(1 + \frac{1}{\psi}\right)\sqrt{\sqrt{8} kT} \frac{\Gamma C_D}{f_T}BW_{3dB}$$
 Figure of merit

- Input referred rms noise is proportional to BW_{3dB}^{1.5}
 - This means that both R_F noise and MOS noise have the same dependence from the TIA bandwidth
 - It is possible to demonstrate that, after noise optimization, the fraction of $i_{n,TIA}^{rms}$ originating from the FET is $\sqrt{\Psi}$, while the fraction coming from feedback resistor R_{F} is $\sqrt{1-\psi}$

Noise and bit rate

- Bandwidth (BW_{3dB}) is proportional to bit rate (ISI)
- Input referred mean square noise current is proportional to BW_{33dB}
- Noise performance degrades so quickly when bit rate increases?
 - Yes, if we use the same technology (f_T) and photodiodes (C_D)
 - No, if we use better technology and lower cap photodiodes
- Usually we have
 - f_T increases linearly with bandwidth (bit rate)
 - C_D is proportional to $\frac{1}{\sqrt{BW_{3dB}}}$
- Under this assumption we have that

 $i_{n,TIA}^2 \propto bit \ rate$

Capacitance and responsivity

- TIA noise optimization is a quite complex topic, however it seems that to reduce photodiode capacitance $C_{\scriptscriptstyle D}$ is for sure helpful
 - Integrated photodetectors (Silicon Photonics) shows smaller C_D.
 However their responsivity too is lower than optimized standalone photodetectors

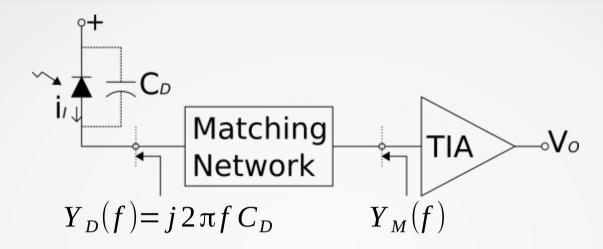
$$\overline{P_{sens}} = Q \frac{\sqrt{\overline{i_{n,TIA}^2}}}{R} \longrightarrow \overline{P_{sens}} \propto \frac{\sqrt{C_D}}{R} \longleftarrow \overline{i_{n,TIA}^2} \propto C_D$$

 Normally, optical links based on integrated photodiodes show a worse sensitivity, because the responsivity degradation effects are not completely compensated by lower capacitance C_D

Low Noise Techniques

- Noise performance can be optimized not only acting on device sizing, bias currents and component values
- Circuit topology modifications
 - Noise matching: passive network in between the photodetector and the TIA input
 - Noise canceling: although noise is a random phenomenon, it can be reduced subtracting two voltages or currents with the same noise but complementary signal waveform
 - Bandwidth reduction plus equalizer, to reduce the integrated noise

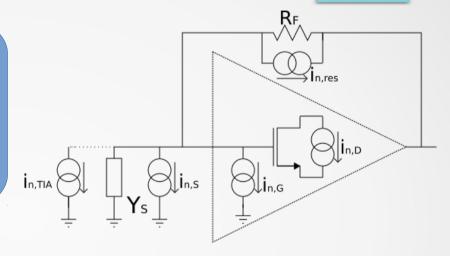
Noise Matching (1/3)



- The admittance Y_D(f) of the photodetector is transformed with a passive network in Y_M(f), for which the TIA produces less noise
 - The noise matching network must minimize the noise current referred to intrinsic PD in the bandwidth of interest
 - The combination of noise matching and TIA must exhibit a flat frequency response Z_T(f) from intrinsic PD to TIA output in the bandwidth of interest

Noise Matching (2/3)

Input noise equations have been calculated assuming capacitive impedance at TIA input. What happens when the impedance is a generic Y_s(f)?



G_s(f), the real portion of Y_s(f), generates noise itself

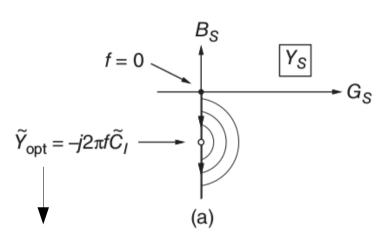
$$I_{n,TIA}^{2}(f) = 4kT|G_{S}(f)| + \frac{4kT}{R_{F}} + 2qI_{G} + 4kT\gamma g_{d0} \frac{[G_{S}(f) + 1/R_{F}]^{2} + [B_{S}(f) + 2\pi f\widetilde{C}_{I}]^{2}}{g_{m}^{2}}$$
Feedback resistor

FET channel noise

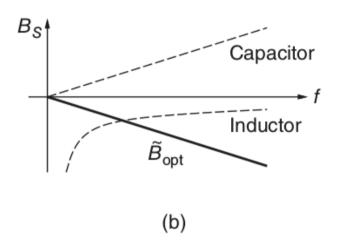
Gate shot noise

Real part of the source impedance

Noise Matching (3/3)



Optimum source impedance at a given frequency

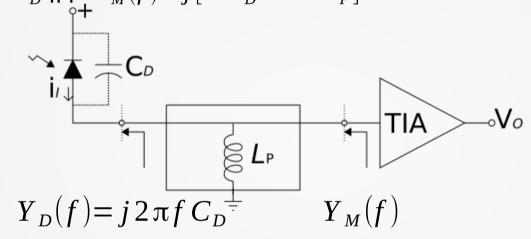


Trajectory of frequency dependent optimum in the source—admittance plan

- A negative capacitance in parallel to the photodetector would be ideal
- Noise matching networks typically achieve a perfect match for only a couple of discrete frequencies

Shunt inductor (1/2)

• The inductor transforms the photodetector admittance $Y_D(f) = j \omega C_D \operatorname{in}_+ Y_M(f) = j [\omega C_D - 1/\omega L_P]$



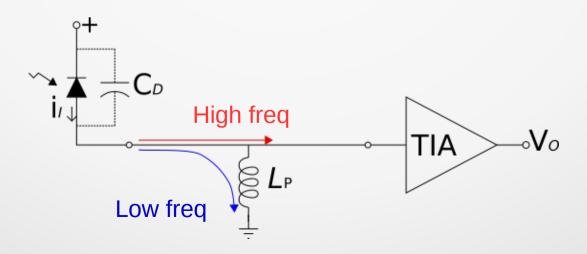
Perfect noise matching is achieved when

$$Y_{M}(\omega) = \widetilde{Y}_{opt}(\omega) = -j \omega \widetilde{C}_{I} \rightarrow L_{P} = \frac{1}{\omega^{2}(C_{D} + \widetilde{C}_{I})}$$

 The optimum inductance is frequency dependent, thus a perfect match happens at a single frequency

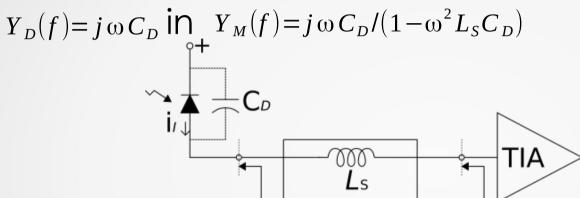
Shunt Inductor (2/2)

- Is shunt inductor technique good enough?
 - The fact that it conceptually works only at a given frequency is not the main limitation
 - Unfortunately, a shunt inductor makes the whole transfer function band-pass, making it unsuitable for receivers of broadband signals



Series Inductor (1/2)

The inductor transforms the photodetector admittance



$$G^2 = g_m^2 / (\gamma g_{d0} R_F) + 1/R_F^2$$

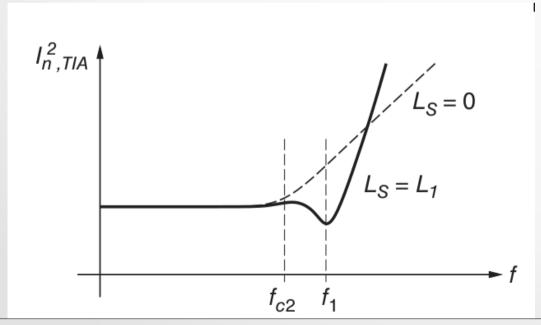
Perfect noise matching is achieved when

$$Y_{M}(\omega) = Y_{opt}(\omega) = -j\omega \widetilde{C}_{I} \rightarrow L_{S} = \frac{1}{\omega^{2}C_{D}} \frac{\omega^{2}(C_{D} + \widetilde{C}_{I})\widetilde{C}_{I} + G^{2}}{\omega^{2}\widetilde{C}_{I}^{2} + G^{2}}$$

Low-pass response, with single freq optimum

Series Inductor (2/2)

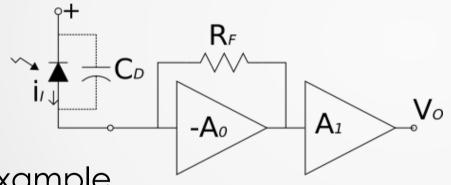
- Like the shunt inductor, noise can be minimized only at single frequency
- This approach becomes appealing if we try to minimize noise at a frequency where noise raises proportionally to f²



PSD clearly reduced around f₁ Not so evident that the sensitivity (integral of PSD) is better

TIA with post amplifier (1/2)

 To break the transimpedance limit, it is possible to add a post amplifier with gain A₁, boosting the overall transimpedance of the same factor A₁



$$R_T = A_1 \frac{A_0 R_F}{A_0 + 1}$$

- Example
 - R_F =500 Ω , A_0 x f_A =44 GHz, A_1 =2, BW_{A1} =22 GHz (same technology)

$$ightharpoonup R_{\tau}=1 k\Omega$$
, BW=6.5 GHz

$$BW_{3dB} = \sqrt{\sqrt{2-1}} BW_S$$

Cascade of Butterworth filters

TIA with post amplifier (2/2)

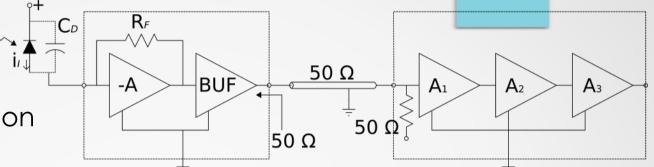
- We can achieve even higher transimpedance trading gain for bandwidth at A₁, but with a bandwidth reduction
- A new transimpedance limit exists

$$R_{T} < \sqrt[4]{\left(\sqrt[n+1]{2} - 1\right)^{n+2}} \frac{\left(A_{0} f_{A}\right)^{n+1}}{2\pi C_{T} B W_{3dB}^{n+2}}$$

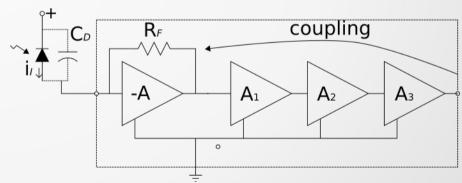
- In most situations the second factor grows faster than the first one shrink, leading to a net gain in transimpedance over a TIA without post amplifier.
- Why spend time and energy to optimize the transimpedance of the shunt feedback TIA, while we can easily add a post amplifier to boost it?
 - For noise reasons: R_F has to be maximized because its noise is inversely proportional to its value

Single chip solution? (1/4)

 Transmission line for broadband connection and matching



- High power consumption because of buffer and termination
- High cost and board complexity
- More compact solution, with significant power saving compared to the two-chips solution



- The swing at amplifier output is very high and there is a lot of noise
- Such a noise can be injected back to sensitive TIA input

Single chip solution? (2/4)

- The following coupling mechanisms in an integrated TIA
 + MA can be found
 - Capacitive coupling between metal traces, bond pads and package pins
 - Coupling through chip substrate
 - Coupling though the inductance and resistance of shared power and ground connections
 - Magnetic coupling between bond wires.

Single chip solution? (3/4)

- To minimize coupling, the following techniques may be used
 - Place the input and output pads as far apart as possible, ideally on opposite sides of the chip
 - Use differential signaling and symmetric placement of the associated traces and pads
 - Use a buried-layer shield under sensitive input pads to reduce substrate coupling
 - Surround the TIA and MA blocks by shield rings (e.g., substrate contacts or isolation trenches) and separate the blocks by about 100 to 400 µm to reduce lateral substrate coupling

Single chip solution? (4/4)

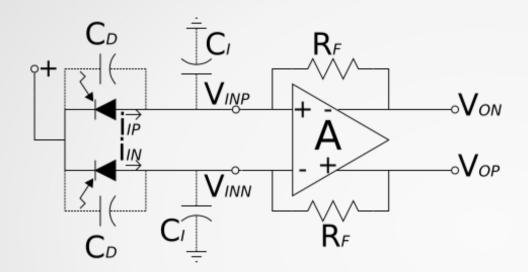
- Mount the (thinned) chip with a conductive glue on a ground plane to provide a good (vertical) substrate connection to an external ground
- Use separate power and ground pads for the TIA, MA, and output buffer blocks and use on-chip decoupling capacitors to avoid coupling through the power network
- Use an on-chip voltage regulator for the sensitive TIA block to reduce the supply coupling
- Keep ground bond wires short and use double bonding, if possible, to minimize their inductance. Arrange critical bond wires at right angle to minimize magnetic coupling.

Differential TIA (1/2)

- When TIA and MA are integrated in a SOC and in multichannel receivers, the use of differential topologies is a good choice
 - Immunity to power supply and substrate noise
 - Rejection of parasitically coupled signals
- Additionally (at the cost of a current penalty) they provide
 - Higher linearity* (lower even order distortion products)
 - Higher voltage swing

^{*} Although never mentioned before, linearity, measured in term of THD, is an important spec in TIA design

Differential TIA (2/2)



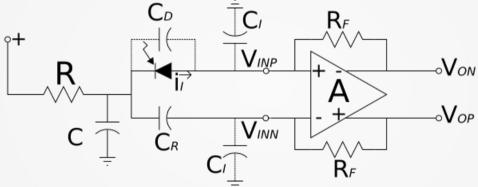
$$V_{OP} - V_{ON} = R_T (I_{IP} - I_{IN})$$

$$R_{T} = \frac{V_{OP} - V_{ON}}{I_{IP} - I_{IN}} = \frac{A_{0}}{A_{0} + 1} R_{F}$$

- The two matched photodetectors present a balanced input impedance
 - Any noise on power supply or the substrate couples equally to minus and plus pin of the amplifier, being thus suppressed by the CMRR

Balanced differential TIA with one PD

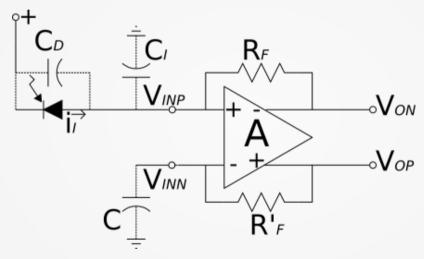
 Many receivers rely on only a single photodetector, for cost saving: how to use a differential TIA with one PD?



- One photodiode is replaced with a replica capacitor C_R , to match capacitance C_D
- For best noise immunity, PD and $C_{\rm R}$ must be connected to the same supply node, through an RC filter

Unbalanced differential TIA (1/2)

 Replica cap C_R can be replaced by a huge cap, if noise immunity is not a primary concern



- Close to a single ended topology
- R'_F noise does not contribute to output noise, thus allowing for better sensitivity

Unbalanced differential TIA (2/2)

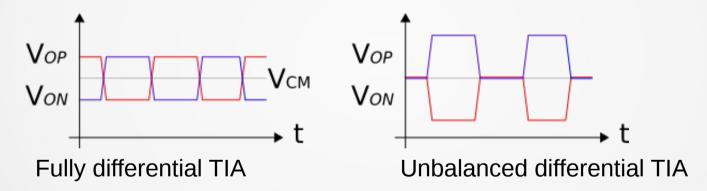
- Only one output provides feedback, but both output nodes are swinging in a complementary way
 - Differential transimpedance is twice the single ended one

$$R_T = \frac{\Delta \left(V_{OP} - V_{ON} \right)}{\Delta I_i} \approx 2 R_F$$

- Less immunity to power-supply and substrate noise
- If the amplifier has been designed for balanced systems, its bandwidth, in unbalanced mode, is lower

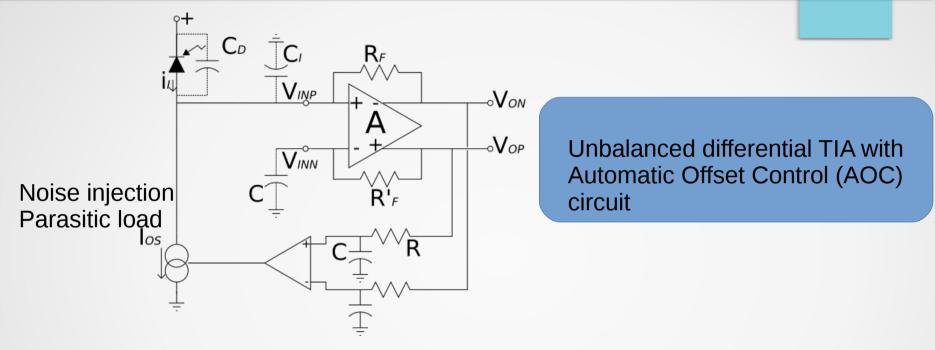
DC input current control

 While the ideal differential TIA effectively shows perfectly balanced output waveform, with no offset, any other implementation suffers of output offset, with limitations at output swing



- Systematic offset voltage limits the maximum possible output swing
- A mechanism to compensate for systematic offset has to be introduced

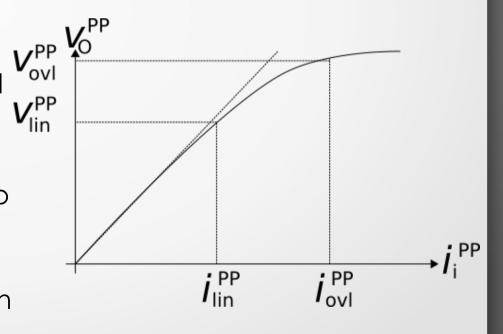
Automatic Offset Control



- The feedback control circuit determines the output offset voltage by subtracting the time average value of the two output signals and controlling the I_{OS} current
- In steady-state I_{os} equals the average photocurrent
- The control loop must be sufficiently slow to prevent the output signals from drifting when long runs of zeros or ones are received

TIA with adaptive transconductance

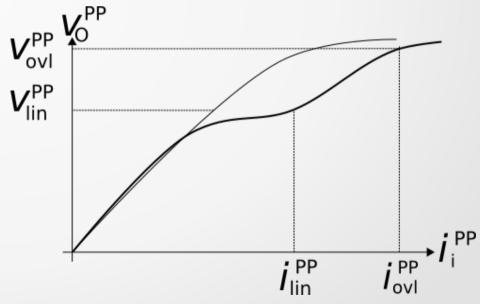
- Noise → SNR → BER→ Sensitivity (minimum amplitude of the input current that can be "managed" by the TIA to guarantee a given BER)
- What about max input current?
 - Starting with a small input current, the TIA output voltage swing v_0^{PP} increases proportional to the input current swing i_1^{PP}
 - Eventually the voltage amplifier starts to compress and the TIA no longer responds linearly $(i_{fin})^{PP}$
 - Going further, we reach the overload limit, with high distortion



Extended linear operation

$$i_{I,\,ovl}^{PP} = v_{O,\,ovl}^{PP} / R_T$$

- The max input current for linear operation as well the input overload current can be pushed to higher values by reducing the transimpedance for higher values of input currents
 - Low input currents: max gain
 - Input current approaching linear operation: transimpedance reduced (by a control loop)
 - Beyond a given limit, the control loop cannot reduce the gain, and an increase of the input current causes distortion



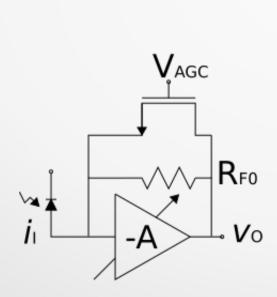
Variable TIA transimpedance

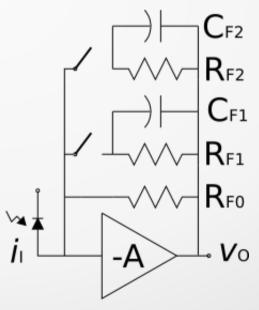
- The impedance of a shunt feedback TIA can be controlled by
 - Varying the feedback resistance R_F
 - Shunting a variable amount of photodetector current away from the input
 - Attenuating the photodetector current by a variable amount
- More in general, whatever is the TIA topology, an additional variable gain amplifier can be added

Variable Feedback Resistance

$$R_T = \frac{A_0 R_F}{A_0 + 1}$$

- The feedback resistor may be varied
 - Continuously, in response to a control voltage V_{AGC}
 - Discretely, in response to a digital code





TIA with continuous control

- The feedback resistor is implemented with a MOS operating in the linear regime
- A fixed resistor R_{FO} in parallel improves the linearity and limits the maximum resistance
- The gate of the MOS transistor is driven by the gain control circuit, providing
 - Low V_{AGC} voltage when a small input current is present (high feedback resistance → high gain)
 - High V_{AGC} voltage when an high input current is present (low feedback resistance → low gain)

TIA with digital control

- The maximum feedback resistor is reduced by switching additional resistors R_{F1} , R_{F2} ...in parallel to it
- A digital control allows for a wider and more precise transimpedance tuning range
 - R_{on} of transistor used in analog control may significantly change over corners, while resistors match better (if R_{on} of single switches is negligible)
- It requires a digital controller

Stability and bandwidth control (1/2)

$$Q = \frac{\sqrt{(A_0 + 1)R_F C_T T_A}}{R_F C_T + T_A}$$

- R_F plays a significant role in the TIA loop stability
 - Reducing it while keeping the amplifier (A₀ and T_A) fixed pushes the TIA towards the instability

$$f_I = \frac{1}{2\pi R_F C_T} \longrightarrow \qquad \qquad f_A = \frac{1}{2\pi T_A}$$

Dominant pole

 Moreover TIA bandwidth may change, accordingly to the desired gain setting, thus impacting on system performance (overshooting, eye-opening, noise)

Stability and bandwidth control (2/2)

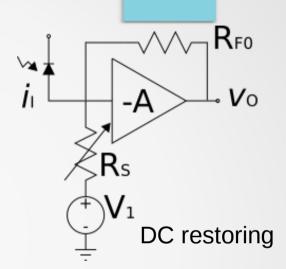
- One way to keep the TIA bandwidth approximately constant is to reduce the gain of the voltage amplifier, proportional to the feedback resistor
- Assuming A₀ x f_A constant (technology dependent) we get

$$A_0 \propto R_F \longrightarrow f_A \propto 1/A_0 \longrightarrow f_A \propto 1/R_F$$

- Both $f_{\rm I}$ and $f_{\rm A}$ move together and the open-loop pole spacing remains fixed, and the close-loop bandwidth is independent on R_F value
- Hard to track amplifier gain and R_F value

Variable input shunt resistor

- For large optical signals R_s is reduced to divert some of the photodetector current to ground, thus preventing from overloading the TIA
- For weak optical signals, R_s is increased such that almost all photodetector current flows into the TIA (no sensitivity degradation)

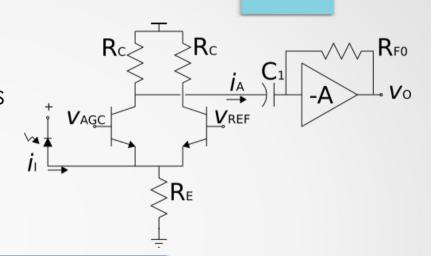


$$R_{T} = \frac{A_{0} R_{F}}{(A_{0}+1) + R_{F}/R_{S}}$$

- Varying the shunt resistor R_s has the advantage, over varying the feedback resistor $R_{\scriptscriptstyle F}$, that it is easier to maintain stability and constant bandwidth
- More robust to overload current (not flowing through the amp)
- R_s is realized through a FET (added capacitance at input node)

Variable input attenuator

- Current attenuator in between the photodetector and the TIA
- The AC current from the photodetector is splitted in two branches
 - i_A flows into the TIA
 - $-i_1 i_A$ is damped into the power rail



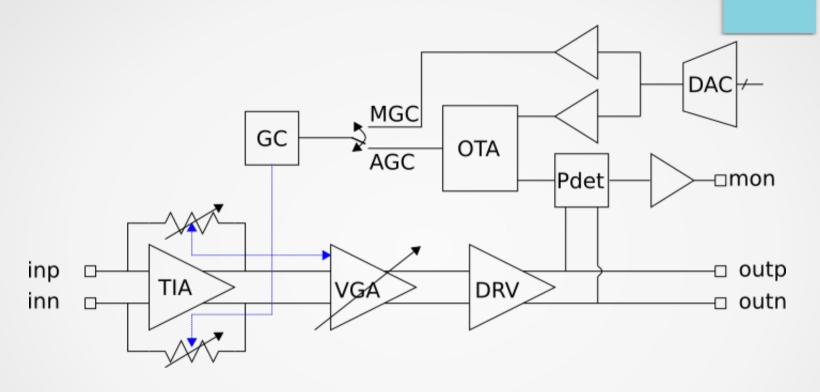
$$R_{T} = \frac{1}{1 + \exp\left[\left(V_{REF} - V_{AGC}\right)/V_{T}\right]} \frac{A_{0}R_{F}}{A_{0} + 1}$$

- Drawback: the DC voltage drop across R_C varies with the control voltage
 - To prevent the attenuator from disturbing the TIA's operating point AC coupling capacitor C₁ is inserted

AGC and MGC

- Once identified the way to control the transimpedance gain of an optical receiver, the following operation conditions can be set
 - Automatic Gain Control (AGC): based on a "feedback", the circuit reacts to a change in the input current amplitude, adapting its gain to have a constant amplitude output signal
 - Manual Gain Control (MGC): the circuit is open loop and works at a fixed gain value. A variation in the input current amplitude is automatically translated in a variation of the output voltage amplitude (although a loop may be closed through the digital circuits)

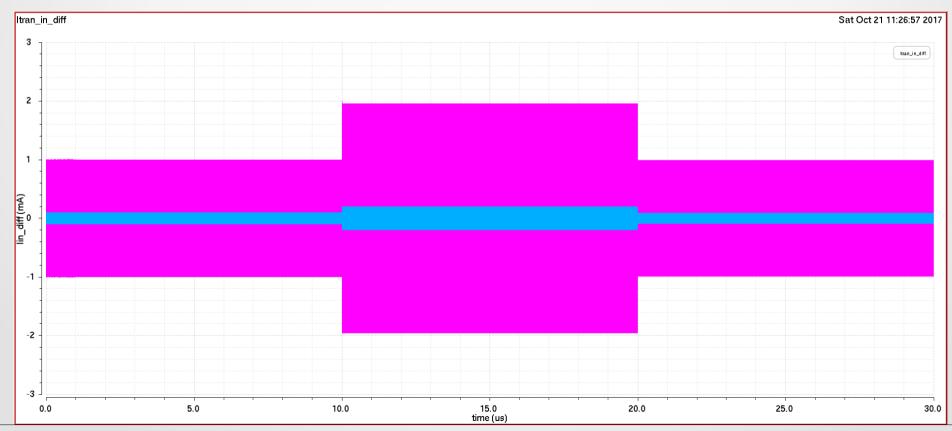
Automatic Gain Control



- AGC: through DAC the desired output voltage is set, and the loop reacts automatically setting the right gain (acting on TIA and VGA).
- MGC: through DAC the desired gain of the chain is set

AGC vs time: input currents vs time

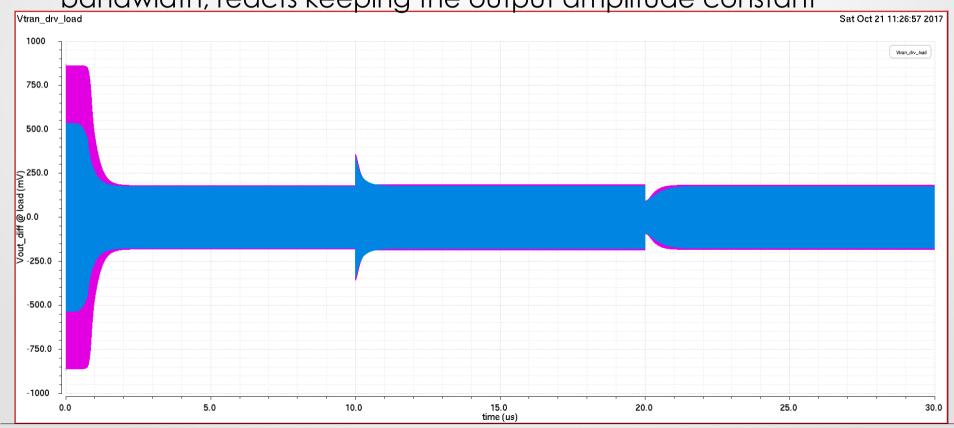
- 0 <t <10µs: iin=200µA ppdiff, iin=2mA ppdiff
- 10 µs<t <20µs: iin=400µA ppdiff, iin=4mA ppdiff
- 20 μs<t <30μs: : iin=200μA ppdiff, iin=2mA ppdiff



AGC vs time: output voltages

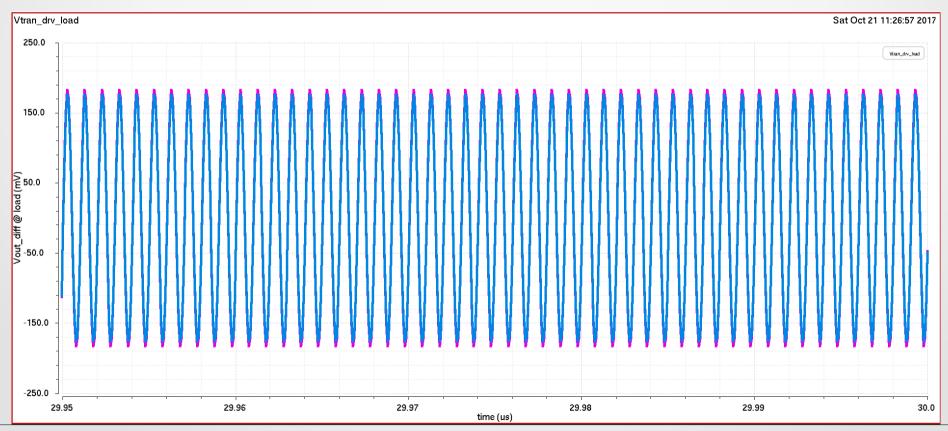
 After the startup, the loop forces the output voltage to the desired amplitude

 At 10 and 20 µs, the loop, in a time inversely proportional to the bandwidth, reacts keeping the output amplitude constant



AGC vs time: output voltages (zoom)

- After a short transient, the output amplitude is exactly the same, although the input currents are significantly different
- The gain settles to different values



AGC vs time: control voltages

- The control voltage Vgc changes lowering the gain when the input current amplitude increases
- The Pdet output monitors the amplitude of the output signal



Shunt feedback TIA limitations

- Shunt feedback TIA are widely used, although trade-offs and criticity have been highlighted
- The major issue for a shunt feedback TIA, preventing their use in a specific type of applications, is the dependence of both bandwidth and stability on the photodetector parasitic cap

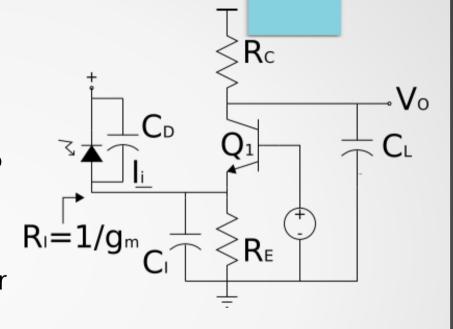
$$\omega_0 = \sqrt{\frac{A_0 + 1}{R_F C_T T_A}}$$

$$Q = \frac{\sqrt{(A_0 + 1)R_F C_T T_A}}{R_F C_T + T_A}$$

 In applications where the TIA has to work with a variety of photodetectors exhibiting a wide range of capacitances, this dependence can be problematic

Common base/gate TIA (1/3)

- Low input impedance $(R_I \approx 1/g_m)$, pushing the input pole to high freq
- The photodetector current I_i flows almost unattenuated through Q1 into collector resistor $R_{\rm C}$
- Q1 acts as a unity gain current buffer with an input impedance much lower than its output impedance



$$R_E \gg 1/g_m$$

$$g_0 \ll 1/R_C$$

$$R_b \ll 1/g_m$$

$$Z_{T}(s) = \frac{R_{T}}{(1+s\omega_{p1})(1+s\omega_{p2})}$$

with
$$R_T = R_C$$

$$\omega_{p1} = \frac{g_m}{C_T}$$

$$\omega_{p2} = \frac{1}{R_C C_L}$$

Common base/gate TIA (2/3)

- Common base TIA has two poles transfer function
 - ω_{p1} : corresponding to input node
 - ω_{p2} : corresponding to output node
- The same transfer function is achieved using a common gate MOS TIA, where g_m is replaced by $g_m + g_{mb}$ (body effect)
- This TIA, is called feedforward TIA, or open loop TIA; it is simple but suitable for low power applications, but not for low noise

Common base/gate TIA (3/3)

Second order effects

– A finite emitter resistor R_{E} or a finite current gain β diverts some of the photodetector AC current away from R_{C} , resulting in a lower transimpedance and a lower input impedance

$$R_T = R_C/(1 + g_m/R_E + 1/\beta)$$
 $R_I = 1/(g_m + 1/R_E + g_m/\beta)$

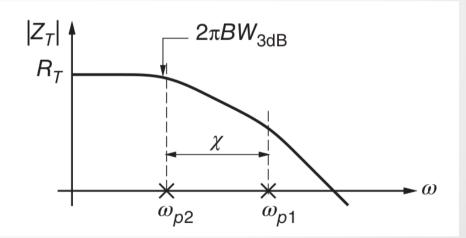
- $R_{\rm E}$ and β impact also on the input pole, making it faster $\omega_{\rm p1} = (g_{\rm m} + 1/R_{\rm E} + g_{\rm m}/\beta)/C_{\rm T}$
- A non zero output conductance g₀ increases the input resistance

$$R_{I} = 1/g_{m}(1+g_{0}R_{C})$$

Bandwidth considerations

• To make the TIA's bandwidth insensitive to the photodetector capacitance, the input pole $\omega_{\rm p1}$ has to be at a higher frequency than the output pole $\omega_{\rm p2}$

 $BW_{3dB} \leq \omega_{p2}/(2\pi)$



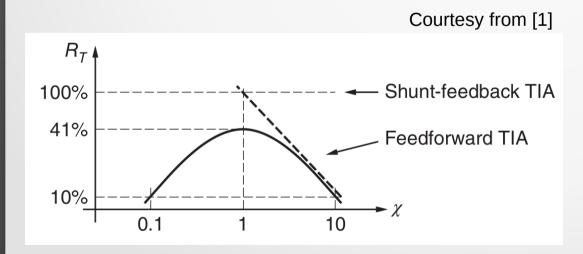
• Ideally $\chi = \omega_{p1}/\omega_{p2}$ has to be higher than 10 to make BW_{3dB} practically not dependent on C_D value

Common base transimpedance limit

 The concept of transimpedance limit may be applied to common gate topology too

$$R_T \leq \frac{A_0 f_A}{2\pi C_T \chi BW_{3dB}}$$

The equality is reached only for large values of χ . Moreover, as we increase the pole spacing to decouple the bandwidth from C_D , the maximum achievable transimpedance is linearly reduced



The transimpedance reaches its maximum for $\chi=1$, with a value equal to 41% of the shunt feedback limit. Given the same bandwidth and technology a CB TIA has a lower transconductance than the corresponding shunt feedback

CB TIA: input referred PSD

- To calculate the input referred noise current PSD we need to find the transfer function from the noise sources back to TIA input
- Under these hypothesis:

$$(g_m R_E)^2 \gg \beta$$
 $R_E \gg R_B$ $g_m R_C \gg 1$

$$i_{n,TIA}(f) = \frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_c}{\beta} + 2qI_c \frac{(2\pi C_T)^2}{g_m^2} f^2 + 4kTR_B (2\pi C_D)^2 f^2$$

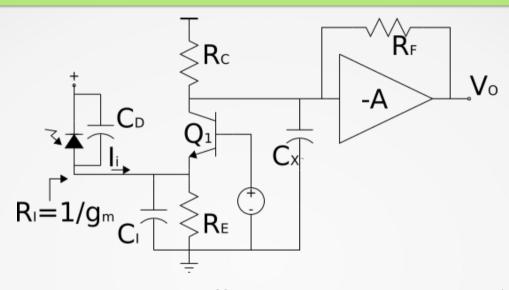
- The noise expression is similar to that of the shunt-feedback TIA with common emitter input stage: the main differences are
 - R_C now plays the role of R_F
 - New noise term due to bias resistance R_F

 R_{B}

Example (Common base TIA)

	Symbol	10 Gbps	40Gbps
Transition frequency	f _T	79.5 GHz	318 GHz
Gain x Bandwidth	$A_0 f_A$	44 GHz	177 GHz
PD capcacitance	C _D	0.15 pF	0.075 pF
Input capacitance	C	01pF	0.05 pF
Transconductance	9 _m	50 mS	100 mS
Load resistor	R _C	123 Ω	61.7 Ω
Input pole freq	f_{p1}	31.8 GHz	127.4 GHz
Output pole freq	f_{p2}	7.17 GHz	28.7 GHz
Pole Spacing	X	4.44	4.44
Transimpedance	R _T	123 Ω	61.7 Ω
Input Impedance	R _I	20 Ω	10 Ω
3 dB Bandwidth	BW _{3dB}	6.85 GHz	27.4 GHz

Shunt Feedback TIA with input CB



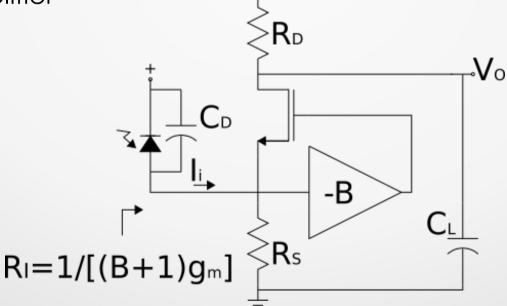
- The common base current buffer can also be combined with the shunt feedback TIA
 - To still be "insensitive" to photodetector capacitance
 - To have better noise performance than common-gate only
 - As a drawback, power consumption increases significantly
- The CB stage is loaded by the input impedance of the shunt feedback stage ($R_F/(A_0 + 1)$), much lower than R_C

Regulated cascode TIA (1/3)

 Although common base TIA can be realized also with MOS transistors (common gate), usually the higher transconductance achievable, for a given current, with BJTs make CB architecture more appealing and efficient than CG

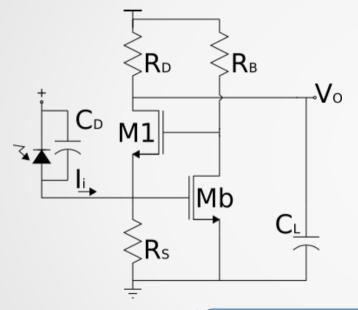
 The Regulated Cascode topology is an alternative way to increase MOS transconductance, without increasing current, but adding a

boosting amplifier



Regulated cascode TIA (2/3)

The amplifier B can be easily implemented through MOS transistor



The booster amplifier is realized with a common source MOSFET stage, Mb and $R_{\mbox{\tiny B}}$, with the following DC gain

$$B_0 = g_{m,Mb} R_B$$

• Assuming the boosting stage with a single pole (at $1/T_B$), zero output impedance and infinite input impedance, we get [1]

$$Z_{T}(s) = R_{T} \frac{1 + s/\omega_{z}}{[1 + s/(\omega_{0}Q) + s^{2}/\omega_{0}^{2}][1 + s/\omega_{p2}]}$$

$$R_T = R_D \qquad \omega_z = \frac{B_0 + 1}{T_B} \qquad \qquad \omega_{p\,2} = \frac{1}{R_D C_L} \qquad \qquad \omega_0 = \sqrt{\frac{(B_0 + 1) \, g_{m1}}{C_T + C_B}} \qquad Q = \frac{\sqrt{(B_0 + 1) \, C_T \, g_{m1} \, T_B}}{C_T + B_0 C_M + g_{m1} \, T_B}$$

Regulated cascode TIA (3/3)

- $C_T = C_D + C_I + C_M$: total input capacitance
 - C_D: photodetector capacitance with all parasitic capacitances
 - C_i: input capacitance of the booster amplifier plus C_{sb1}
 - C_M: C_{gs1}+ C_{gdB}
- Low frequency transimpedance and output pole are coincident with common gate TIA
- The input pole is different and it is substituted by a (complex) pole pair given by ω_0 and Q, and a zero at ω_z
- The zero and the complex pole could potentially result in a peaked frequency response and, even worse, in an instability. As a general rule, a Q around 1/sqrt(2) is recommended

Regulated cascode TIA bandwidth

• Assuming Q=1/sqrt(2) and ω_z at high frequency, regulated cascode TIA bandwidth can be calculated [1]

$$f_{b1} = \omega_0 / (2\pi) = \sqrt{\frac{g_{m1}}{2\pi C_T} B_0 f_B \frac{B_0 + 1}{B_0}} \approx \sqrt{\frac{g_{m1}}{2\pi C_T} B_0 f_B}$$

- $\frac{g_{m1}}{2\pi C_T}$: input cutoff frequency of the unboosted common-gate
- $B_0 f_B$: gain-bandwidth product of the booster stage
- Adding a booster amplifier speeds-up the bandwidth of the input node to approximately the geometrical min of its bandwidth before boost is applied and the gain bandwidth product of the boosting amplifier

Transimpedance limit

- A transimpedance limit, under the constraint Q=1/sqrt(2) can be found for regulated cascode TIA too
- Additional hypothesis are
 - Gain bandwidth product of common-gate and boosting stage equal
 - ω_z close to infinite

$$R_T \leq \frac{(A_0 f_A)^2}{2\pi C_T \chi^2 BW_{3dB}}$$

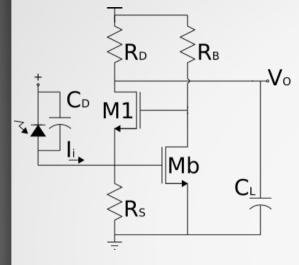
$$\omega_{b1} = 2\pi f_{b1}$$

$$\omega_{p2} = \frac{2\pi A_0 f_A}{(g_{m1} R_D)}$$

$$\omega_{b1} = \chi \omega_{p2}$$

 Significantly better than common-gate TIA: the addition of a booster stage permits a reduction of M1 width without loss in bandwidth.
 Smaller M1 means smaller load capacitance C_L, permitting a larger drain resistor RD, and thus a larger transimpedance

Input referred noise PSD



- Simplifying assumptions (approximations)
 - $R_S \rightarrow \infty$, $g_{mb,M1} = 0$, $g_{d0,M1} = g_{d0,Mb} = 0$, $C_{gd,M1} = 0$
- − K_S → ¬¬¬¬, 9_{mb,M1} − σ, 9_{d0,M1} 9_{d0,Mb} σ, 9_{ga,M1}
 − M1 and Mb induced gate noise negligible
 - Referring all noise sources to the input we get

$$I_{n,TIA}^{2}(f) = \frac{4kT}{R_{D}} + \frac{4kT}{R_{S}} + 4kT \widetilde{\Gamma_{M1}} \frac{\left[2\pi \left(\frac{C_{D} + C_{I}}{B_{0} + 1} + C_{M}\right)\right]^{2}}{g_{M1}} f^{2} + 4kT \widetilde{\Gamma_{Mb}} \frac{B_{0}^{2}}{(B_{0} + 1)^{2}} \frac{\left[2\pi \left(C_{D} + C_{I}\right)\right]^{2}}{g_{Mb}} f^{2} + \frac{4kT}{R_{S}}$$

$$C_{M} = C_{gs,M1} + C_{gd,Mb} \qquad C_{I} = C_{sb,M1} + C_{gs,Mb} \qquad \Gamma_{M1} = \gamma_{M1} (g_{d0,M1}/g_{m,M1}) \qquad \Gamma_{Mb} = \gamma_{Mb} (g_{d0,Mb}/g_{m,Mb}) \qquad B_{0} = g_{m,Mb} R_{B}$$

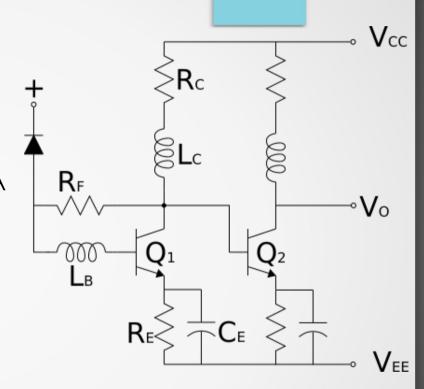
- The first term is smaller than in common gate TIA because higher values of R_D are permitted, while the second one is exactly the same
- The third term is reduced by a factor ($B_0 + 1$) while the fourth one is new

Some TIA example from literature

- If you go to IEEE Explorer Digital Library and look for TIA papers, you'll
 get hundreds of results; here, just as example, a short list of TIA
 examples found in literature is listed
 - K. Vasilakopoulos, S. P. Voinigescu, P. Schvan, P. Chevalier, and A. Cathelin. "A 92GHz bandwidth SiGe BiCMOS HBT TIA with less than 6dB noise figure", Proceedings of IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pages 168–171, October 2015 [13]
 - H.H.Kim, S.Chandrasekhar, C-A-Burrus and J.Bauman, "A Si BiCMOS transimpedance amplifier for 10-Gb/s SONET receiver", IEEE Journal of Solid-State Circuits, SC-36(5): 769-776, 2001[14]
 - S.Smohan, M.D.M Hershenson, S.P.Boyd and T.H.Lee, "Bandwidth extension in CMOS with optimized on-chip inductors", IEEE Journal of Solid-State Circuits, SC-35(3): 346-355, 2000 [15]
 - C.Kromer, G.Sialm, T.Morf, M.L.Schmatz, F.Ellinger, D.Erni and H.Jackel, "A low-power 20 GHz 52 dBΩ transimpedance amplifier in 80 nm CMOS", IEEE Journal of Solid-State Circuits, SC-39(6), 885-894, 2004 [16]

SiGe BiCMOS HBT High Speed TIA

- Shunt feedback TIA optimized for high speed
 - Single transistor (Q_1) voltage amplifier with resistor load R_C
 - Emitter degeneration R_E to improve TIA linearity
 - Feedback resistor R_F to close the loop
 - On chip inductors L_B and L_C to boost the bandwidth
 - Shunt capacitor C_E to improve high frequency response and suppress the noise of R_E
 - Common emitter buffer stage (Q₂)



№. Vasilakopoulos, S. P. Voinigescu, P. Schvan, P. Chevalier, and A. Cathelin. "A 92GHz bandwidth SiGe BiCMOS HBT TIA with less than 6dB noise figure", Proceedings of IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pages 168–171, October 2015

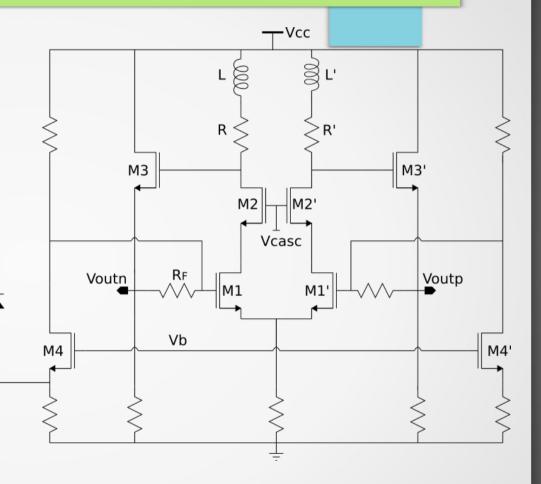
Differential TIA with inductive input coupling

- Signal path with BJT, bias network with MOS transistors Shunt feedback architecture R_F' RF Voutp 01 Q1' Voutn L2 L2' L1 L1' 000 MM 000 М1 M2' M2' Cp' Ср
 - The gain is provided by the differential pair Q1 and Q1' and the resisstor load R and R'
 - Constant current provided by M1 and linear load → constant common mode output voltage
 - LC coupling network to improve noise performance

H.H.Kim, S.Chandrasekhar, C-A-Burrus and J.Bauman, "A Si BiCMOS transimpedance amplifier for 10-Gb/s SONET receiver", IEEE Journal of Solid-State Circuits, SC-36(5): 769-776, 2001

TIA with common-gate input stage

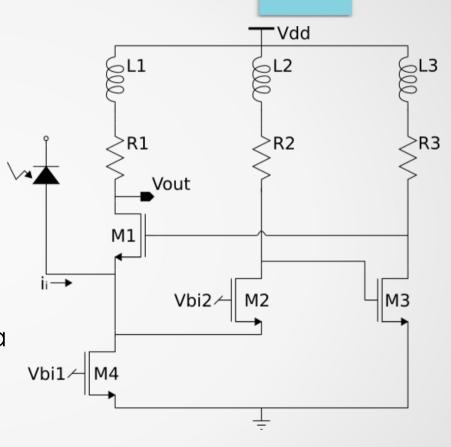
- This design combines two common gate input stages with a conventional shuntfeedback
- Shunt peaking inductors L and L' broaden the bandwidth of the shunt-feedback stage
- M4 implements the common gate input stage, decoupling the PD capacitance from the critical node at the gate of M1



S.Smohan, M.D.M Hershenson, S.P.Boyd and T.H.Lee, "Bandwidth extension in CMOS with optimized on-chip inductors", IEEE Journal of Solid-State Circuits, SC-35(3): 346-355, 2000

Low voltage regulated cascode TIA

- Regulated cascode TIA for short optical links
- Two stage booster stage (M₂ R₂ / M₃ R₃) to give more room to transistor M1, whose gate, in a conventional regulated cascode TIA, should be two Vgs above ground
- The two stage boosting amplifier provides more gain thus resulting in a lower TIA input resistance

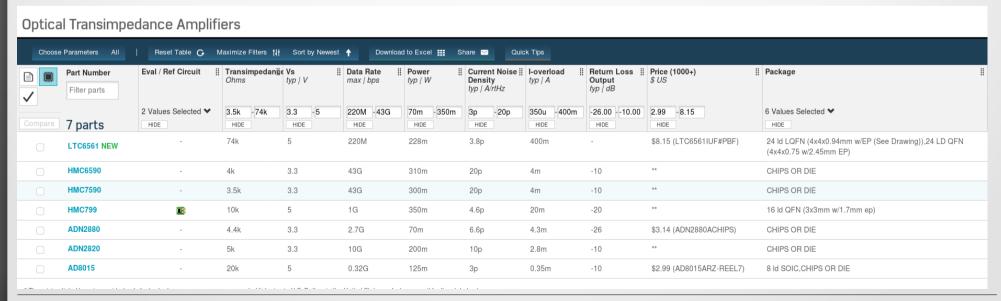


C.Kromer, G.Sialm, T.Morf, M.L.Schmatz, F.Ellinger, D.Erni and H.Jackel, "A low-power 20 GHz 52 dBΩ transimpedance amplifier in 80 nm CMOS", IEEE Journal of Solid-State Circuits, SC-39(6), 885-894, 2004

Some TIA example (1/3)



Analog Devices optical TIAs offer a complete, high performance, single chip solution for converting photodiode current into a differential voltage output. "Supporting data rates from 155 Mbps to 11.1 Gbps, our transimpedance amplifiers are ideally suited for data communications and telecommunications applications supporting lay protocols including 1×, 2×, 4×, and 8× Fibre Channel, 10GBASE-LX4, SONET/SDH up to OC-192 with FEC, and 10 Gigabit Ethernet."



Some TIA example (2/3)



- QORVO: it is an American semiconductor company that designs, manufactures, and supplies radio-frequency systems and solutions for applications that drive wireless and broadband communications. It comes from the merging of Triquint Semiconductor and RF Microdevices
- QORVO's transmipedance amplifiers (TIAs) are high-efficiency, dielevel solutions that support key requirements for 100 to 400 Gb/s optical networks. "Our product line serves both the transmit and receive portions of high performance optical networks"

 Transimpedance Amplifiers (4) 			Export to Excel Expansion								
		Description A *	Bandwidth ‡ GHz	Small Signal Gain ♣ dB	Differential Transimpedance Gain & ohm	Differential Output Vpp ♣ mV	Equivalent Input Noise & PA/rtHz	Voltage [♣] ∨	Current ∳ mA	Package Type 🕏	Package mm
	Compare Parametric Filters ∨										
	☐ TGA4871	Quad Limiting Transimpedance Amplifier	16 to 30		6,000	900	15	2.7 to 3.5	130 to 190		
	☐ TGA4872	32 Gb/s Dual Linear Transimpedance Amplifier with AGC	30		100 to 7,500	200 to 900	20	3.3	186		
	☐ TGA4874	32 Gb/s Quad Linear Transimpedance Amplifier with SPI Control	30		100 to 6,800	200 to 900	20	3.3	344		•
	TGA4875 NEW	100G PAM4 / DMT Transimpedance Amplifier	36		5,400	750	15	3.3	110		1.522 x 1.192 x 0.150

Some TIA example (3/3)



 MACOM: MACOM Technology Solutions is a developer and producer of radio, microwave, and millimeter wave semiconductor devices and components. The company is headquartered in Lowell, Massachusetts. MACOM's optoelectronics products also includes a wide range of transimpedance amplifiers (TIA) for line and client side 10G, 40G and 100G fiber optic receivers. "Our portfolio includes linear TIAs for long haul coherent receivers and limiting TIAs for shorter range NRZ based receivers."

Part Number 1	Ordering 41	Short Description #1	Max Data AT Rate (Gbps)	Differential ITransimpedance Gain (kOhms)	Small Signal ### Bandwidth (GHz)	Input 41 Overload Current (mA)	Input If Referred Noise (IRN, RMS nA) (nA)	Optical sensitivity with PIN (dBm)	Optical IT Sensitivity with APD (dBm)
		V	0.2 56	2 10000	20 35	1.5 4.5	0 1500	-39 -17	-35 -25
M03002	Inquire	28 Gbps Transimpedance Amplifier (TIA)	28		21				
M03100	Inquire	28 Gbps Quad Channel Transimpedance Amplifier (TIA)	28	2.9	22	2.8	1	-17	
M03101	Inquire	28 Gbps Quad Channel Transimpedance Amplifier (TIA)	28		21				
M03102	Inquire	28 Gbps Quad Channel Transimpedance Amplifier (TIA)	28		21				
MATA-003806	Inquire	32 Gbps Dual Channel Linear TIA for DP-QPSK Advanced Receivers	32	10000	25	3	17		
MATA-005817	Inquire	56 Gbaud Single Channel Linear TIA	56	6	35	2	0		
MATA-03003	Inquire	28 Gbps TIA	28	3.8	21	4	1	-18	
MATA-03006	Inquire	28 Gbps Transimpedance Amplifier (TIA)	28	3.8	21	4	1		
MATA-03013	Inquire		28	3.8	21	4	1	-18	
MATA-03802A	Inquire	Dual Channel Linear TIA	32	5	25	2			

A TIA example from ISSCC [17]

A.Awny, R.Nagulapalli, D.Micusik, J.Hoffmann, G.Fischer, D.Kissinger, A.C.Ulusoy,

"A Dual 64 Gbaud 10 kΩ 5% THD Linear Differential Transim pedance Amplifier with Automatic Gain Control in 0.13 um BiCMOS Technology for Optical Fiber Coherent Receivers" 2016 IEEE International Solid-State Circuits Conference



Paper, courtesy from IEEE



Slides, courtesy from IEEE

Outline

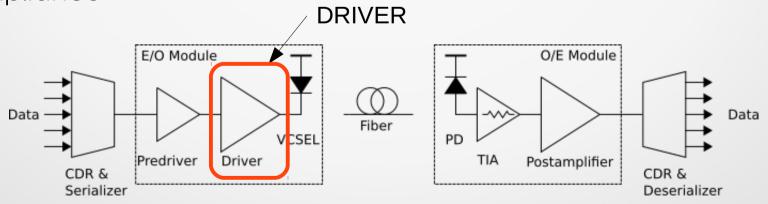
- (Short) Introduction to Optical Communications
- Broadband Techniques
- Optical RFICs
 - Transimpedance Amplifier (TIA)
 - Modulator Driver
- Conclusions

Comparison of LED & Laser

Characteristics	LEDs	Lasers
Output Power	Linearly proportional to drive current	Proportional to current above the threshold
Current	Drive current: 50 to 100 mA pk	Threshold current: 5 to 40 mA
Coupled Power	Moderate	High
Speed	Slower	Faster
Output Pattern	Higher	Lower
Bandwidth	Moderate	High
Wavelengths available	0.66 to 1.65 um	0.78 to 1.65 um
Spectral width	Wider (40-190 nm FVHM)	Narrow (0.0001 to 10 nm FVHM)
Fiber Type	Multimode only	SM, MM
Easy to use	Easier	Harder
Lifetime	Longer	Long
Cost	Low (5 to 300 \$)	High (100 to 10000 \$)

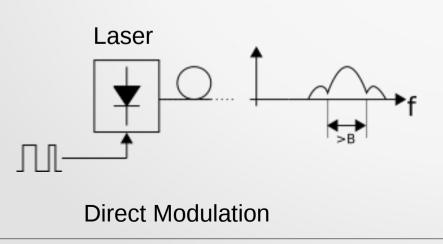
Laser driver

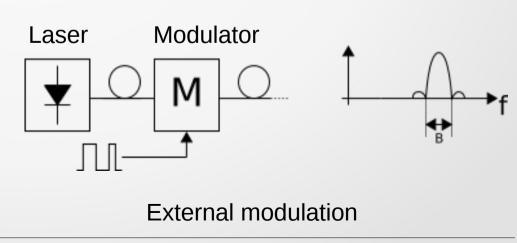
- A Laser driver is the key block in the optical communication TX chain (Electrical to Optical module). It amplifies the RF voltage at its input (usually provided by a predriver) and, in principle, it can be viewed as a simple current switch that turns the laser on and off, according to the logical value of the data [3]
- A driver has to satisfy stringent requirements, mainly related to its speed and linearity, but its design is hard also because of technological constraints in output current capability and voltage compliance



Modulation of optical source

- There are two alternative ways to generate a modulated optical signal
 - Direct modulation: the laser is turned on and off by modulating its current
 - External modulation: the laser is on at all times (CW laser), and the light beam is modulated with a kind of optoelectronic shutter (a modulator)





Transmitter specifications (1/2)

Spectral line-width

- It is the width of its optical spectrum. More precisely, it is the width of the power spectral density of the emitted electric field in terms of frequency, wavenumber or wavelength.
- Also assuming a perfectly monochromatic CW light source, the spectrum of an NRZ modulated signal is roughly wide like the bit rate. The wavelength line-width is then defined as

$$\Delta \lambda = \frac{\lambda^2}{C} \Delta f \approx \frac{\lambda^2}{C} B$$

- Example: $\lambda=1.55$ nm, B=10 Gb/s $\rightarrow \Delta\lambda=0.08$ nm

Transmitter specifications (2/2)

 For most transmitters, the modulation process not only changes the light's amplitude, but also phase and frequency (chirp), thus causing the spectral linewidth to broaden (this is more evident in case of direct modulation)

$$\Delta \lambda \approx \frac{\lambda^2}{C} \sqrt{\alpha^2 + 1} \cdot B$$

 Alpha is called "chirp parameter" or line-width enhancement factor

Extinction ratio

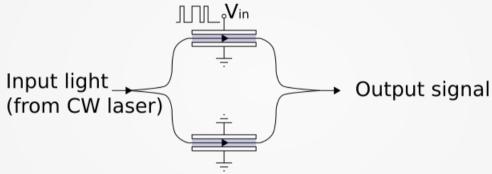
- Optical transmitters do not shut off completely when a zero is transmitted. This effect is captured by the definition of extinction ratio ($ER=P_1/P_0$)

Modulators

- Two types of external modulators are used in coherent optical communications systems
 - Electroabsorption modulator (EAM)
 - Small
 - It can be integrated with the laser on the same substrate
 - Mach Zender modulator (MDM)
 - Larger
 - Superior chirp and extinction ratio characteristics

Mach-Zehnder modulator

 The Mach-Zehnder modulator employs a Lithium Niobate (LiNbO3) crystal, in which the propagation velocity is a function of the electric field across it



- The incoming optical signal is splitted equally and is sent down to two different optical paths; after few cm the two paths recombine, causing the optical waves to interfere with each other
- In LiNbO3 crystal, the propagation velocity is a function of the electric field applied across it. The phase shift experienced by light may be modulated by an electrical signal

Laser and modulator driver

- The laser is an optical device. Where is the boundary between electrical and optical?
 - Direct modulation → laser modulator
 - External modulation → driver modulator
- Both laser and driver modulator are electric circuits (that can be integrated on silicon) that provide, respectively, the laser bias current, and the voltage needed to implement the "modulation"
- Because external modulation allows for best performance (lower chirp degradation) let's focus on driver modulator only

Some example from industry (1/3)



 QORVO: it is an American semiconductor company that designs, manufactures, and supplies radio-frequency systems and solutions for applications that drive wireless and broadband communications. It comes from the merging of Triquint Semiconductor and RF Microdevices

Description	Number of Channels	3dB BW (GHz)	RF Port IN/OUT	Output (Vpp)	Gain (dB)	Voltage (V)	lq (mA)	Part Number
11.3 Gb/s EML Driver, 4x4mm²	1	8	Diff/Diff	1.8-4.5	30	3.3	130	TQP5115
28 Gb/s Differential SMT Modulator Driver	1	25	Diff/Diff	6-9	24	4-5	450	TGA4957-SM
32 Gb/s Differential SMT Modulator Driver	1	27	Diff/Diff	6-9	25	5	428	TGA4959-SL
Wideband Driver Die (Linear or Limiting)	1	37	SE/SE	4-6	11	6-8	215	TGA4852
Low Power Wideband Driver Die (Linear or Limiting)	1	50	SE/SE	1-3	12	2.5-3.3	50	TGA4840
Low Power Wideband Modulator Driver (Linear or Limiting)	1	33	SE/SE	1-3	11	2.5-3.3	50	TGA4840-SM
Low Power Wideband Quad Modulator Driver (Linear or Limiting)	4	30	SE/SE	1.5-2.5	11	2.5-3.3	40-70	TGA4851-SL
Wideband Driver Die (Linear or Limiting)	1	50	SE/SE	1.5-2.5	13	2.5-3.3	40-70	QPA4971D
Wideband Modulator Driver (Linear or Limiting)	1	37	SE/SE	1.5-2.5	13	2.5-3.3	40-70	QPA4971
Low Power Wideband Quad Modulator Driver (Linear or Limiting)	4	30	SE/SE	1.5-2.5	13	2.5-3.3	40-70	QPA4854
32 Gb/s Optical Modulator Driver	1	27	SE/SE	4-9	32	6	485	TGA4943-2-SL
32 GBaud Quad Linear Driver	4	25	Diff/SE	3-5	26	3-5	-	TGA4899-SL
32 GBaud Quad Linear Driver with Equalization	4	27	Diff/SE	3-5	28	3-5	-	QPA4961*
64 GBaud Quad Linear Driver	4	45	Diff/SE	4.5	27	3-5	-	QPA4964*
64 GBaud Quad Linear Driver with Equalization	4	45	Diff/SE	4.5	27	3-5	-	QPA4964A*
64 GBaud Quad Linear Driver Die with SPI	4	45	Diff/Diff	2.5-3.5	20-25	3-5	-	QPA4963D*

Some example from industry (2/3)

Partners from RF to Light

MACOM: is a new breed of analog semiconductor company-one that delivers a unique combination of high growth, diversification and high profitability. "We are enabling a better-connected and safer world by delivering breakthrough semiconductor technologies for optical, wireless and satellite networks that satisfy society's insatiable demand for information".

Part Number 👢	Ordering 11	Short Description #1	Linear/Limiting #1	Max. Data- Rate (Gbps)	Input Voltage - Min (mVpp)	Number of Channels	Rise/Fall Time 41 (ps)	Output Unit Voltage - Max. (Vpp)	Supply Voltage (V)
			<u> </u>	11.3 46	400 700	•	12 27	1.6 5	-5.2 6
MAOM-001201	Inquire	11.3 Gbps EML Driver Die	Limiting	11.3	400	1	27	2.3	3.3
MAOM-002200	Inquire	28 Gbps EML Driver	Limiting	28	500	1	12	2.5	-5.2
MAOM-002203	Inquire	28 Gbps EML Driver	Limiting	28	500	1	12	2.5	4.3
MAOM-002207	Inquire	28 Gbps EML Driver Die	Limiting	28	500	1	12	2.5	4.3
MAOM-003115	Inquire	28 Gb/s Linear EA Modulator Driver IC	Linear	28	600	1		2	3.6
MAOM-003401	Inquire	Low Power, Quad Channel 28Gbps EML Driver	Limiting	28	700	4	12	1.6	3
MAOM-003418	Inquire	Quad Channel 46Gbps Linear Modulator Driver	Linear	46	450	4		5	6
MAOM-02204A	Inquire	Quad Channel 28Gbps EML Driver	Limiting	28	500	4	12	2.5	4.3
MAOM-03409D	Inquire	32 Gb/s Linear Differential Modulator Driver IC	Linear	32	700	4			
MAOM-03417B	Inquire	Quad Channel 32 Gbps Linear Modulator Driver	Linear	32		4	12	4.5	5

Some example from industry (3/3)

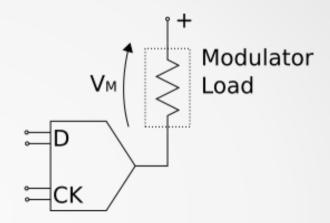


Inphi's industry leading drivers for 100G to 600G coherent technologies provide cutting edge performance, quality and reliability to enable the exponential acceleration of big data transmissions for long haul and metro applications. Drivers take an encoded signal from DSP and amplify electrical data to high voltages for transmission over optical lines. "Our drivers enable applications covering distances of 100m to 1000 Kms at data rates up to 600G. This includes drivers for high performance Mach-Zehnder modulators, externally modulated lasers (EML) and directly modulated lasers (DML)."

Part 🔺 No.	Product Type	Market Segments	\Rightarrow
IN3214HG	Modulator Drivers 32 Gbps Quad Mach-Zehnder Modulator Driver	Long Haul/Metro	
IN3214SZ	Modulator Drivers 32 Gbps Quad Linear Mach-Zehnder Driver	Long Haul/Metro	
IN3215SZ	Modulator Drivers 32 Gbps Quad Linear Differential-Input, Single-Ended Output Driver with SMT Interface	Long Haul/Metro	
IN3216DZ	Modulator Drivers 32 Gbps Quad Differential Linear Mach-Zehnder Modulator Driver	Long Haul/Metro	
IN3217SZ	Modulator Drivers 4 x 32 Gbps Quad Linear Differential Inputs, Single-Ended Output Driver in LGA Package	Long Haul/Metro	
IN4514SZ	Modulator Drivers 45 Gbps Octal Linear Differential Input, Single-Ended Output Driver with SMT Input Interface and G3PO Output Interface	Long Haul/Metro	
IN4517SZ	Modulator Drivers 45 Gbaud Quad-Channel, Linear Mach-Zehnder Modulator Driver in LGA Package	Long Haul/Metro	

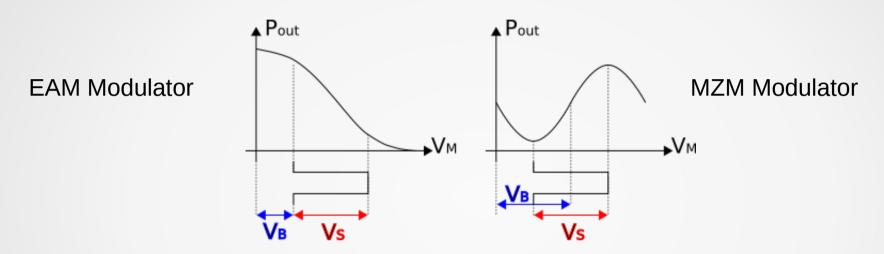
Modulation and bias voltage (1/3)

- A single ended modulator driver shows
 - Differential data at input
 - An (optional) clock input
 - A voltage V_M(t) at the output, across the modulator
 - Additional control signals



- The modulation voltage V_s is the difference between the "on" and "off" state voltage supplied to the modulator driver $(V_s = V_M^{PP})$
 - EAM driver: the bias voltage (or DC offset voltage), V_B , is the voltage supplied by the driver during the "on" state
 - MZM driver: V_B is the average voltage supplied by the driver

Modulation and bias voltage (2/3)



- EAM modulator: the output voltage swing must be equal or larger than the modulators's switching voltage V_{sw} , to obtain a sufficient extinction ratio (ER)
- MZM modulator: the output voltage swing must closely match the switching voltage $V\pi$; ER degrades if the voltage swing is smaller or greater than $V\pi$ because of the sinusoidal switching curve (undermodulation or overmodulation)

Modulation and bias voltage (3/3)

- The optimum bias voltage for MZM (assuming On-Off keying) is at the midpoint of the switching curve, also known as the "quadrature point"
- Because of paths mismatch and drift, the quadrature point is not known a priori; usually an automatic bias controller (ABC) is used to generate V_{B}
- The required voltage swing often dictates the driver technology. For example, whereas a 3 V swing usually can be attained with a SiGe technology, a 5 V swing may necessitate a GaAs techology

Voltage swing

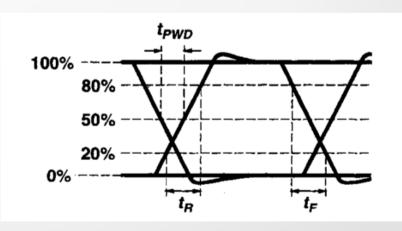
	V _s [V]
EAM modulator	$0.2 < V_s < 3$
MZM modulator	$0.5 < V_s < 5$

Bias voltage

	V _B [V]
EAM modulator	$0 < V_B < 1$
MZM modulator	$0 < V_{B} < 10$

Rise and fall time

- The rise time (t_R) and fall time (t_F) of a modulator driver output voltage can be measured in the electrical (oscilloscope) or optical domain (O/E converter + oscilloscope)
 - t_R is measured from the point where the signal has reached 20% of its full value to the point where it has reached 80%
 - t_F is measured, similarly from the 80% to the 20% point
- The rise and fall time must both be shorter than one unit interval (UI), to avoid ISI
 - For an NRZ system usually the total system rise time has to be lower than 0.7 UI (including fiber rise time and RX rise time)



(courtesy from [2])

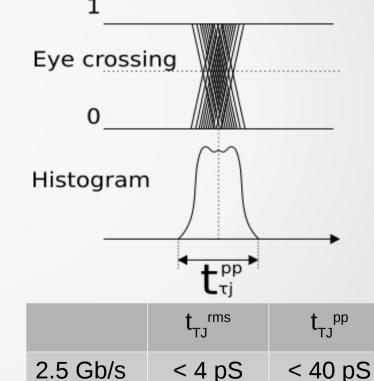
Pulse width distortion

- An offset or threshold error in the driver circuit may lengthen or shorten the electrical output pulses relative to their ideal width of one UI
- The deviation of the pulses from their ideal width is known as pulse-width distortion (PWD) and its amount t_{PWD} is defined as the difference between the wider pulse and the narrower pulse, divided by two.
- A low t_{PWD} is desirable because it improves the horizontal eye opening and helps in RX Clock and Data Recovery (CDR). Many modulator drivers contain a Pulse Width Control (PWC)

	t _{PWD} (without PWC) [pS]	t _{PWD} (with PWC) [pS]
2.5 Gb/s	< 20	< 16
10 Gb/s	< 5	< 4

Jitter generation

- As already discussed, data signals in a receiver not only suffer from PWD, but also from timing jitter. Some of this jitter is produced in the transmitter, and is known as the jitter generation
- Jitter in the electrical output signal is caused by noise and ISI from the driver circuit, and also by reflections on interconnects
- A lower jitter generation is desirable because it improves the horizontal eye opening and make the clock-recovery process at the receiver more robust
- Typical values for transmitters are 0.01 UI rms and 0.1 UI peak-to-peak



10 Gb/s

< 1 pS

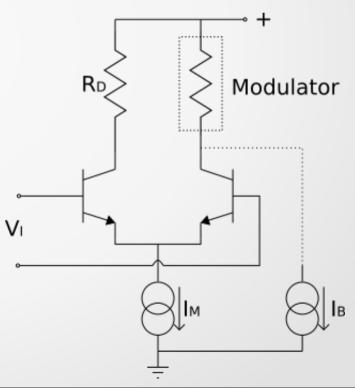
< 10 pS

Driver circuit concepts

- Whatever is the practical implementation, given the characteristics a driver has to present, its design has to be based on the following concepts
 - Current steering output stage
 - Back termination
 - Predriver
 - Pulse-width control
 - Data retiming
 - Automatic bias control
 - Analog modulator driver

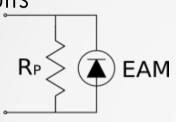
Current steering output stage

- The output stage of most modulator driver is based on the current steering circuit (both BJT or MOS)
- When driving a differential load (like the dual driver MZM), both outputs are used
 - The differential design is insensitive to input common-mode noise and power/ground bounce
 - Total power supply constant (no matter if a 0 or a 1 is transmitted), but it is twice than necessary
 - The voltage across the tail-current source I_M is set by the input CM voltage
 - The modulation voltage can be easily controlled varying the tail current

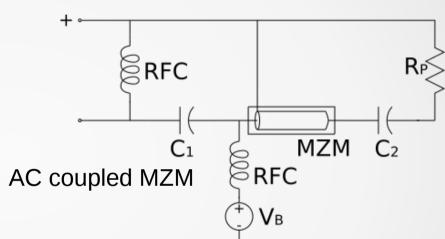


Modulator loads

 Both EAM and MZM modulators may be driven by current-steering circuits

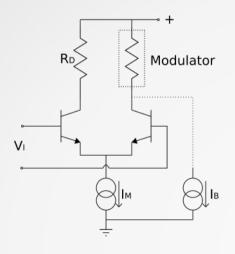


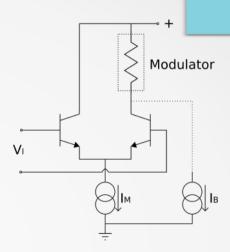
DC coupled EAM



- DC coupled EAM: the parallel resistor R_P converts current into voltage: $V_S = R_P \times I_M$ (modulation voltage)
- AC coupled MZM: pull up inductor followed by AC coupling; $V_s = R_P$ x I_M , where R_P is the MZM termination resistance
 - The bias voltage V_B is applied to the modulator through a bias T
 (RF choke + AC coupling C₁)

Dummy load





- The purpose of the dummy load is to increase the symmetry of the output stage. In fact asymmetric load configuration results in
 - Input offset voltage → PWD
 - Undesirable modulation of the voltage across the tail current
 - In presence of parasitic cap, overshoot can be caused
 - Undesirable current variation
 - Impact on the pre-driver symmetry (two unequal Miller caps) → kick back noise at its inputs

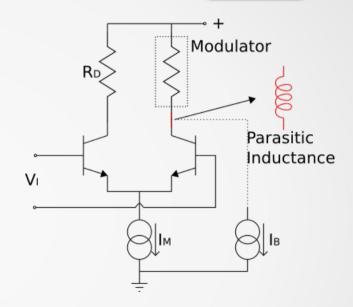
Switching speed

- Current steering circuits, to work for high speed drivers, need to be very "fast"
 - BJT implementation: emitter area has to be large enough to avoid critical current density (Kirk effect), but not too large, to minimize input and output caps
 - MOS implementation: channel length as short as possible, but not too short, to avoid drain-source breakdown voltage. MOS width has to be large enough to ensure full switching at a given input voltage swing, but not too large, to minimize input and output capacitances
- Electromigration issues for interconnection too: the output time constant of the driver increases with the maximum output swing.
 Larger voltages require larger transistors and wider metal traces

Back termination (1/2)

- The connection between the driver output and the modulator may be
 - On-chip traces
 - **Bondwires**
 - Flip-chip connections
- The current flowing in this connections is high and fastly switching
- Whatever is the implementation, the parasitic inductance associated with the connection line causes a voltage drop across it, and possibly ringing too

causes a voltage drop across it, and possible
$$\Delta v(t) = L_{par} di/dt$$



Back termination (2/2)

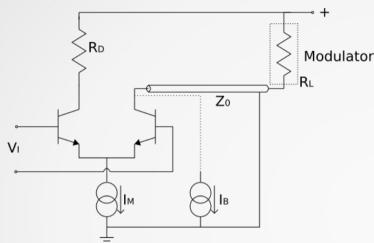
- For high-speed drivers where the load is more than few mm far away, a transmission line is mandatory
 - The parasitic wire inductance is counterbalanced by a distributed cap, to make the characteristic impedance real

$$Z_0 = \sqrt{\frac{L_{par}}{C_{par}}}$$

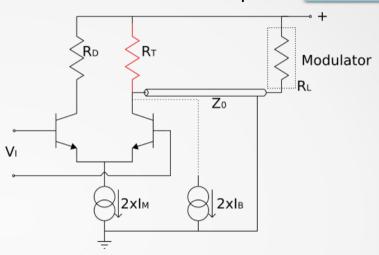
 If a transmission line is used to connect the driver to the modulator, undesiderable reflections may occur. To avoid reflections from the load end of the transmission line back into the driver, the modulator must be matched to the characteristic impedance of the transmission line

Passive back termination

Open collector driver

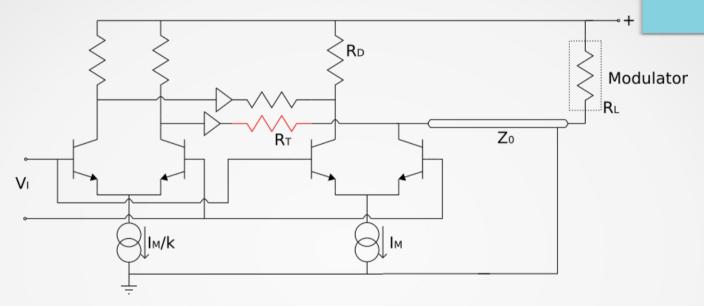


Back terminated open collector driver



- Modulator impedance may be bias dependent → some power is reflected back to the driver
- If the driver shows an high impedance
 - Double reflections → extinction ratio, jitter degradation
- Adding termination resistance R_T (= Z_0) eliminates double reflections
 - Power hungry: only half of the tail current reaches the load

Active back termination

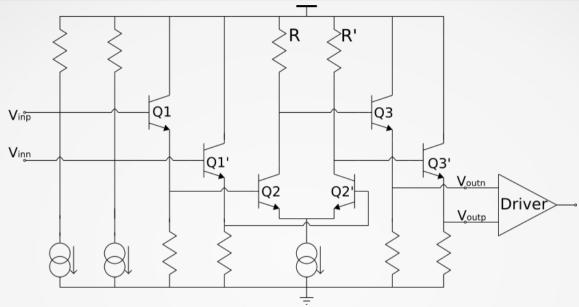


- Active back-termination is a method to avoid double reflections without doubling power consumption
 - The back termination $R_{\scriptscriptstyle T}$ is connected to an AC voltage generated by a replica stage
 - No power is wasted in the back termination R_T (the voltage at the two resistor nodes is always the same)

Pre-driver

- Driver may deliver up to hundreds of mA to the modulator load.
 Output transistor size has to be large enough → Input capacitance may be quite large
 - On chip driving of output transistor at fast speed may be impossible
 - Off chip driving could work, but input return loss of output stage may be critical to be achieved
- Another trade-off sizing driver MOS output stage is about input cap and switching voltage
 - Small devices means small cap but higher switching voltages
 - Big devices means big cap but lower switching voltages
- Usually a pre-driver is generally used to drive the output stage

Pre-driver: an example



- Emitter followers Q3 and Q3' provide the necessary low impedance to drive the driver output stage at high speed
 - Emitter follower output impedance may be inductive: attention has to be payed, to avoid ringing or oscillations
- Q2 and Q2' constitutes the gain stage, with lower tail current and smaller transistor size than output stage
- Q1 and Q1' work as level shifter and additionally reduce the input cap

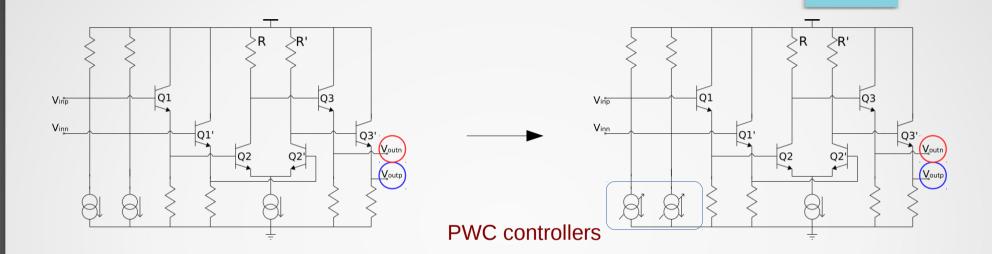
Pre-driver design techniques

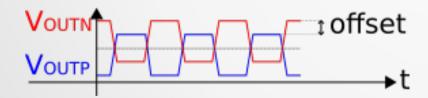
- Predrivers are usually designed using some of the already discussed broadband techniques
 - Feedback techniques
 - Series feedback (emitter/source degeneration)
 - Shunt feedback
 - Cascode transistor
 - Interstage reduction techniques
 - Interstage buffer (emitter follower)
 - Negative capacitance
 - Inductive techniques
 - Inductive load (shunt peaking)
 - Inductive interstage network (series peaking, T-Coil)

Pulse-width control (1/2)

- Pulse-width control need to be implemented in modulator drivers to compensate for pulse-width distortion, generated by offset or by asymmetry between turn-on and turn-off delay of the modulator itself
- Most of the pulse-width controllers operates by introducing a variable offset at the input of the pre-driver
 - It compensates for the random offset voltage of the pre-driver itself (offset loop)
 - It predistorts the electrical output signal such that after electrical to optical conversion the optical pulses are free of PWD

Pulse-width control (2/2)





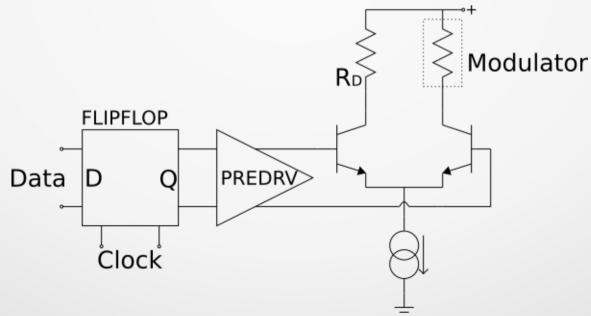


 Two adjustable current sources introduce the variable offset voltage and the subsequent current steering circuit in the predriver acts as the limiter

Data retiming (1/2)

- In high speed modulator drivers, the input data signal is often resynchronized with a clean clock signal before being fed to the predriver
 - Data retiming eliminates pulse width distortion and jitter from the input signal

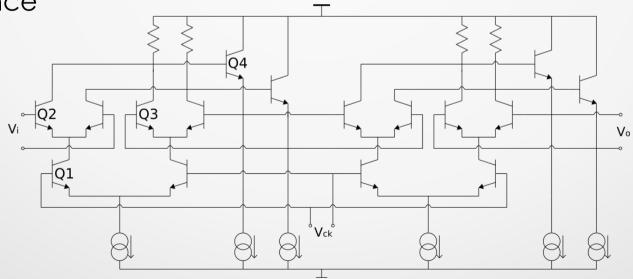
However the clock signal jitter directly appears at the driver



output

Data retiming (2/2)

- Retiming flip-flops are usually implemented with Current-Mode Logic (CML)
 - High speed
 - Low sensitivity to common mode and power-supply noise
 - Constant supply current → minimization of power and ground bounce

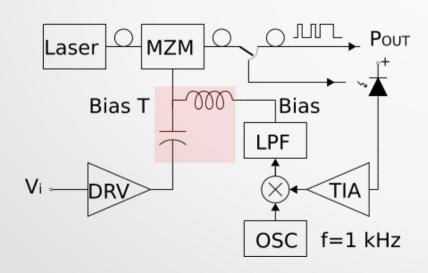


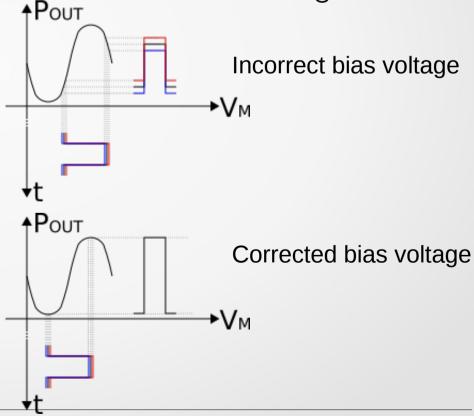
Automatic bias control

 Since the switching curve of Mach-Zender modulators suffers from voltage drift with temperature and age, an Automatic Bias Control (ABC) mechanism usually is required to obtain stable operations

The driver output voltage swing is modulated with a small signal low-

frequency tone (pilot)

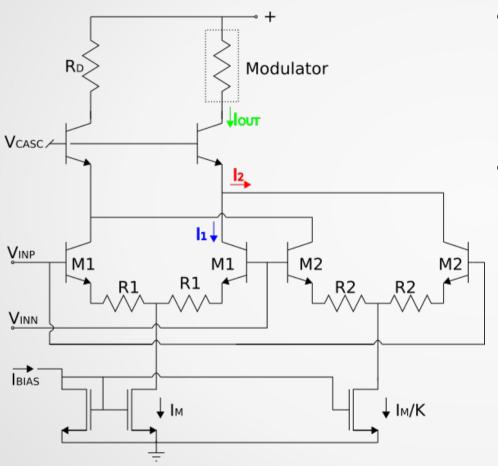




Linearity requirements

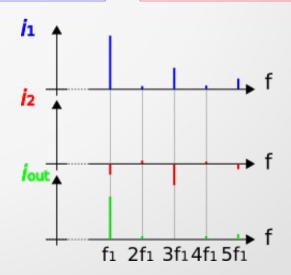
- While noise may be considered the "hot" spec for TIA, linearity is a key issue in the transmission path, when max optical power has to be delivered
- Linearization techniques may be applied both in optical domain (at EAM or MZM level) or in electrical domain
 - Optical feedforward linearization
 - Predistortion circuits
 - Analog technique for modulator driver linearization
 - Degeneration
 - HD cancellation

IM3 cancellation



- Third order harmonic distortion may be canceled out adding a current, with the same IM3, but with different sign
- Additional stage burns a fraction of the bias current I_M

$$I_1 = (I_M/2) + i_1$$
 $I_2 = (I_M/2K) + i_2$



S. Otaka, M. Ashida, M. Ishi and T. Itakura, "A 10 dBm IIP3 SiGe Mixer with IM3 cancellation technique", IEEE Journal of Solid-State Circuits, Vol. 39, N. 12, Dec. 2004

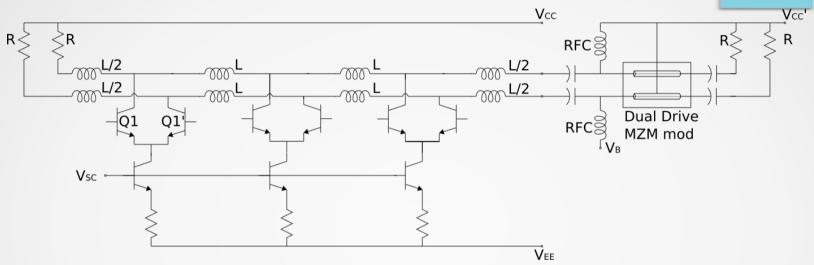
Modulator driver specs (1/2)

Item	Condition	Min	Тур	Max
Ext diff load $[\Omega]$	Load presented between P,N ports	55	65	75
Max data rate [Gbps]		64		
3 dB bandwidth [GHz]		35	40	45
Diff input signal [mV _{ppd}]		200		600
Diff output swing [V _{ppd}]		2	3	4
Max Gain [dB]	$RL_{EXT} = 65 \Omega$	22	24	
Min Gain [dB]			8	
Gain step [dB]			0.3	
Gain variation [dB]	Over temperature (-5 °C < T < 100 °C)			1
THD [%]			3	5
Gain diff between ch [dB]				1
Low Freq. Cutoff [MHz]	Reference frequency 1 GHz		0.5	1
Isolation between ch [dB]		30	40	1

Modulator driver specs (2/2)

Item	Condition	Min	Тур	Max
Input return loss [dB]	0.1 GHz < f < 16 GHz		16	
	16 GHz < f < 24 GHz		12	
	24 GHz < f < EBW		10	
Output return loss [dB]	0.1 GHz < f < 16 GHz			
	16 GHz < f < 24 GHz			
	24 GHz < f < EBW			
CMRR [dB]	0.1 GHz < f < EBW	20		
Power consumption [W]			1.4	1.6
Supply voltage		3	3.3	3.6
Input DC CM [V]	Integrated DC block		0	
Output DC CM [V]			1.65	
# of channels			4	
PKD accuracy [%]	Over temperature (-5 °C < T < 100 °C)	-2		2

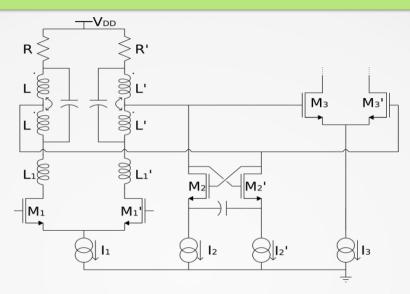
Distributed BJT MZM driver



- The large output cap of transistor can be distributed into an artificial transmission line splitting the current steering transistor pair into n smaller pairs and connecting them with inductors
- The speed is now limited by the cutoff frequency of the transmission lines which can be made high by choosing a large number of sections n

Thomas Y. K. Wong, A1 P. Freuntdorfer, Bruce C. Beggs, and John Sitch. "A 10Gb/s AlGaAdGaAs HBT high power fully differential limiting distributed amplifier for 111-V Mach-Zehnder modulator". IEEE J. Solid-state Circuits, SC-3 1 (10): 1388-1393, October 1996

CMOS pre-driver



- Used in a 10 Gbit/s laser modulator driver realized in 0.18µm CMOS
- Current steering circuit (M₁ and M₁') with series inductor L1, Tcoil and load resistor R and R'
- Negative impedance converter to cancel out load capacitance provided by transistors M_3 and M_3 '

Sherif Galal and Behzad Razavi. "10-Gb/s limiting amplifier and laser/modulator *driver in 0.18-pm CMOS technollogy*". IEEE J. Solid-state Circuits, SC-38 (12): 2334-2340, December 2003

A Driver example from ISSCC

E. Temporiti, G. Minoia, M. Repossi, D. Baldi, A. Ghilioni and F. Svelto

"A 56 Gb/s 300mW Silicon-Photonics Transmitter in 3D-Integrated PIC25G and 55nm BiCMOS Technologies"

2016 IEEE International Solid-State Circuits Conference



Paper, courtesy from IEEE



Slides, courtesy from IEEE

Outline

- (Short) Introduction to Optical Communications
- Broadband Techniques
- Optical RFICs
 - Transimpedance Amplifier (TIA)
 - Modulator Driver
- Conclusions

Conclusions

- So called "Optical" RFICs, such as "TIA" and "modulator drivers" are an hot-topic
 - R&D: looking for technology solutions providing higher performance to accommodate the need for higher speed communications
 - Products: big business, even growing in the next 5/10 years
- Complex topic, requiring different skills: integrated circuit design, communication, system, technology, optics
- If you are inspired by this topic, this is the "momentum"

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